Rail-to-Rail CMOS Voltage Buffer Design for LCD Column Drivers

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***Abstract*— A high–speed rail-to-rail CMOS buffer amplifier with LCD column driver application and a very simple circuit structure, is proposed. The buffer employs a differential FVF at the input stage as a main circuit block as well as a smaller number of transistors compared to many other buffer designs. Advantages of this buffer compared to many others are low quiescent current, very small output impedance and a very small settling time characteristic. The main simulations have been performed using LTSpice with 0.35 µm CMOS technology parameters, whereas the layout is drawn using Microwind. The simulations reveal a result of 0.3 µs in terms of settling time with a power supply of 3.3 V while driving a 1 nF capacitive load and the quiescent current is found to be 3.95 µA. The buffer amplifier is also analyzed in terms of FOM (Figure–of-Merit) performance measure and compared to other previous published buffers, in which the proposed circuit shows an outstanding and better performance. Moreover, the robustness of the proposed circuit to process mismatches and tolerances are verified by Monte Carlo analysis**

***Keywords*— Buffer amplifier, Column driver, Quiescent current, Liquid crystal displays, Settling time**

I. INTRODUCTION

Liquid-Crystal Displays play an important role in portable systems. Column drivers are considered as a significant part of Liquid-Crystal Display (LCD) devices because they contribute to high speed driving, low power consumption and high resolution [1-20]. Large size LCD applications can be found in monitors, desktops, TV, car navigation systems etc. [1-5, 14]. Among the building blocks in LCD column drivers, buffer amplifiers have the main importance within the driver, due to speed capability, voltage swing, resolution, and power dissipation properties it constitutes [6-8]. Since a larger number of output buffers are included on an LCD column driver, the quiescent current has to be kept very small in order to provide low power dissipation. Among the most important parameters of buffer amplifiers are rail-to-rail voltage driving capability, low output impedance and small settling time. The system cost and reliability are directly linked with the number of output drivers, therefore as the number of output drivers is minimized, the system cost is reduced and the reliability increases. Moreover, since a lot of output buffers are integrated in a single chip, it must occupy less layout area to give the opportunity to other output buffers to be integrated in the same chip and the static power consumption should be minimized as much as possible [19]. Another characteristic to be mentioned of output buffers is the static power consumption. In order to extend the battery life-time of flat-panel displays the static power consumption has to be minimized [19]. The input to an output buffer amplifier should be a step-wise function due to pixels which are updated row-by-row [17]. Class B and class AB circuit topologies are the mostly considered topologies for low power buffer amplifier design. Another advantage in comparison to class A is also the small static consumption characteristics they possess [18]. Many output buffer circuits were discussed and shown in the literature recent years for power consumption reduction purpose [1-20]. The circuit in [17] shows low settling time which is considered an advantage since the speed plays an important role in buffer amplifier; but with a drawback in quiescent current which is considered to be very large. In [6] the buffer amplifier has two main drawbacks: it drives too much quiescent current as well as high settling time. Even though the buffer design in [18] shows a good performance in terms of quiescent current with a low value, in contrast the settling time is considered large. Even though Class-B output buffer amplifiers are mostly used for power consumption reduction [3], one main drawback regarding this design is considered to be the large die area due to larger output transistors. Another issue is the high settling time value not capable to drive large LCD panels. Class-AB output buffer amplifiers are candidates to minimize the settling time and power consumption [21-25]. In some cases, there are also class-AB buffer amplifiers which reach good settling time but drive too much quiescent current by using comparator circuits to sense the transient changes in the input [4]. One proposed circuit which has good rail-to-rail performance but high settling time drawback in [1] enables a class B operation. Another circuit which with acceptable quiescent current has been

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proposed but instead it has high settling time [18]. The circuit in [20] has a smaller number of transistors. It shows good performance in terms of settling time with a value of only 0.4µs with a capacitive load connected at the output stage. This circuit has a FOM value of 561.8F/A.s which is mostly affected from the quiescent value which is 4.5 µA and its considered a bit high. The other good case to be mentioned is the buffer in [19] which shows a FOM value of 553.4F/A.s with a good result in terms of settling time; but the main drawback of this circuit is the high value of quiescent current which is 32µA.

In this paper we propose a high-performance rail-to-rail LCD buffer amplifier with a very simple circuit topology implementation, very low settling time and a high performance evaluated in terms of FOM (Figure-of-Merit). In Section 2 we discuss the suggested circuit. Simulations and analysis are discussed in Section 3. In Section 4 the conclusion part is given.

II. THE PROPOSED CIRCUIT

The proposed circuit topology is given in Fig. 1. The circuit applies a differential flipped voltage follower (DFVF) based input stage [8]. The input is applied from the noninverting terminal of the DFVF and the output is fed back to the inverting input of the DFVF. The rail-to-rail operation is provided from NMOS transistors M_3 and M_4 which are the differential inputs. The input signal is applied to the non-inverting terminal whereas the output and the inverting input are tied together as expected from unity gain amplifiers. When the input signal is set to zero, the output voltage will be the replica of the input voltage and it will go down to ground [15]. Transistors M_5 and M_7 form separate common source gain stages. A very high open loop gain is obtained at the output and after applying a negative feedback from the drain terminals of M_9 and M_{10} to the inverting input of the DFVF stage, very small impedance is obtained at the output.

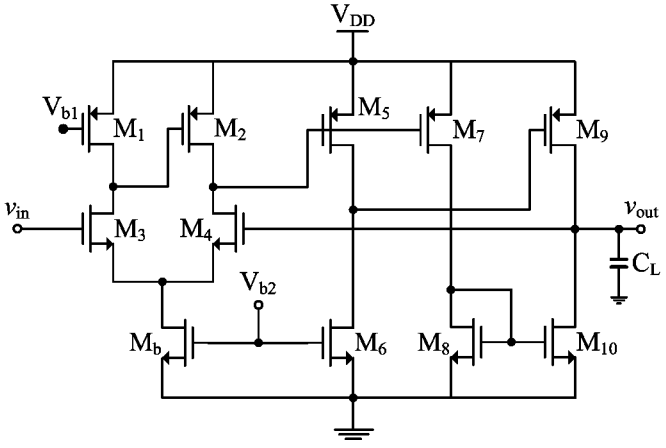

Fig. 1. Circuit schematic of the buffer amplifier

The output impedance value can be given as:

$$R_{out} = 1/\left(g_{m5,7}g_{m3}\right)\left(g_{m9}+g_{m10}\right)\left(r_{o2}\|r_{o4}\right)\left(r_{o5,7}\|r_{o6,8}\right) \quad (1)$$

where g_m and r_o is the transconductance and output resistance of the relevant transistor, respectively.

Transistors M_5 and M_6 form the gain stage. Very high gains are obtained at this stage, so that the value of the feedback factor is increased. As a result of this increase, a very low impedance value is obtained at the output. The charging and discharging currents for the load capacitance are obtained through the transistors M_9 and M_{10}, respectively. Because of this, aspect ratios of these two transistors are kept a bit high compared to other transistors.

III. SIMULATION RESULTS

The introduced circuit is simulated using LTSpice and the 0.35µm CMOS technology parameters provided by Carusone, Johns and Martin (2014). The aspect ratios of the relevant transistors are given in Table 1.

Table I. Aspect ratios of the transistors

Transistor	L [µm]	W [µm]
M_1, M_3	0.9	30
M_2, M_4	0.7	10
M_5, M_7	0.7	30
M_6, M_8	0.7	10
M_9	0.35	150
M_{10}	0.35	50
M_b	0.7	15

The supply voltage is +3.3 V. The biasing voltages are V_{b1} = 2.6V and V_{b2} = 0.8V. The overall quiescent current of the buffer is 3.95 µA. The layout of the buffer circuit which is shown in Fig. 2 is drawn using the finger technique by splitting the long gate of one transistor into two, three or more segments connected in parallel and sharing the same diffusion area of the drain and source contacts [27-29]. The length L dimensions of transistors have roughly values rather than exact values according to the 0.35 µm technology parameter rules in Microwind Software. The measured layout area is found to be 72.6µm x 40 µm = 2904µm^2.

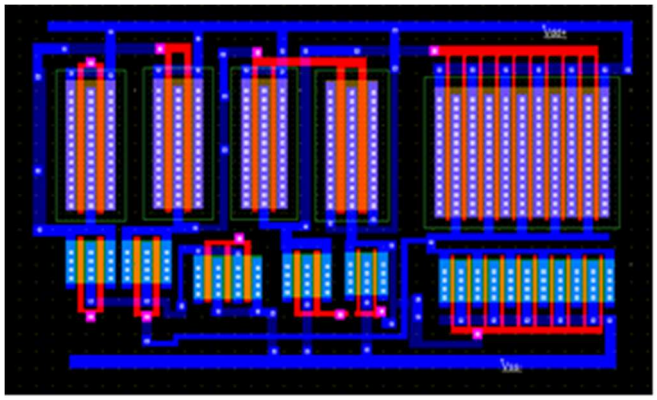

Fig. 2. Layout of the buffer amplifier

In Fig. 3, the output driving capability of the circuit as transient response of the buffer is shown. The buffer is

simulated with a 100 kHz full-swing input step and a load capacitance of 1nF connected at the output. The time-response for a step-wise input shows a result of 0.3 µs in terms of settling time.

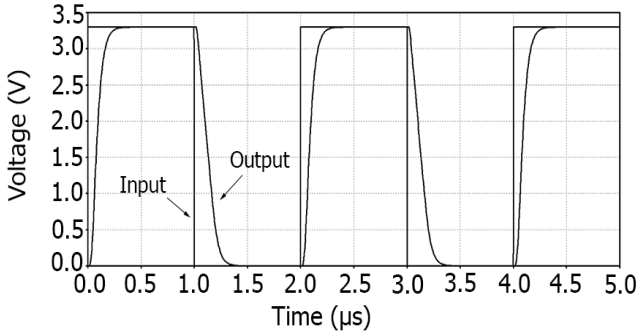

Fig. 3. The transient response of the buffer amplifier driving a capacitive load of C_L=1 nF at the output

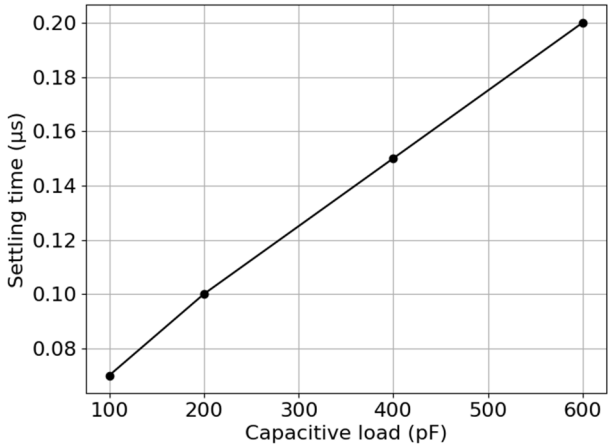

Fig. 4. Transient response for different capacitive load connected at the output

In Fig. 4, we present a stretched view of the buffer in terms of settling time behavior for different capacitive load values connected at the output node. For a capacitive load of 600pF connected at the output, the resulting settling time is 0.2 µs. For 400pF, 200pF and 100pF capacitors, the settling times are found to be 0.15 µs, 0.1 µs and 0.07 µs, respectively. It is obvious that as the capacitive loads decreases, speed of the buffer increases.

In Fig. 5 (a) the frequency response of the amplifier gain is given with a 1nF load capacitance connected. The 3dB frequency is obtained as 22.2 MHz Another frequency analysis is performed for the case with the output left opened and the 3dB frequency is found as 318 MHz as shown in Fig 5 (b).

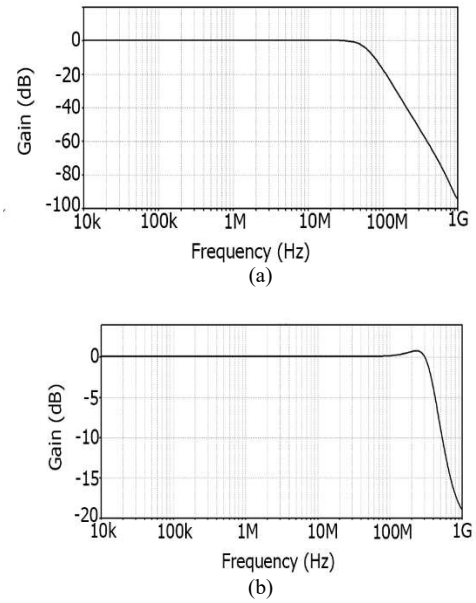

Fig. 5. AC response of the amplifier with capacitive load a) of 1nF at the output and b) without capacitive load

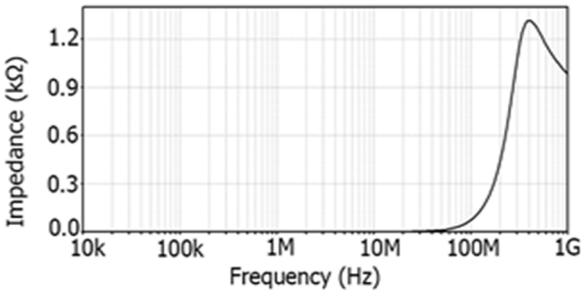

Fig. 6. Output impedance variation with frequency

Fig. 6 shows the simulation results for the output impedance represented in kΩ with respect to the frequency variation. The frequency range is chosen to be between 10 kHz and 1 GHz and the impedance is found as 0.037 Ω at 100 kHz, 0.038 Ω at 1 MHz, 0.5 Ω at 10 MHz and 260 Ω at 100 MHz. From the results it is obvious that the impedance value is small enough to drive capacitive loads effectively as given and expected from Eq. (1).

The circuit is also compared to previously published circuits using the well-known Figure-of-Merit (FOM) value, which was defined as [20]:

$$FOM = \frac{C_L}{I_Q t_s} \tag{2}$$

where C_L is the load capacitance in pF, I_Q is the quiescent current in µA and t_S is the settling time in µs. The higher values of FOM represent exceptional performance.

Table II. Performance comparison of different buffer amplifiers

	Yıldız et al. [18]	**Grasso et al. [17]**	**Grasso et al. [19]**	**Marano et al [10]**	**Arslan [20]**	**This work**
Year	2015	2014	2018	2010	2018	**2020**
CMOS tech. [µm]	0.35	0.5	0.35	0.35	0.35	**0.35**
Vdd [V]	3.3	5	3	3	3.3	**3.3**
C_L [pF]	1000	1000	1000	1000	1000	**1000**
Quies. current µA]	1.6	32	1.63	3.5	4.45	**3.95**
Settling time [µs]	1.45	0.71	1.11	0.9	0.4	**0.3**
In/Out range [%V_{DD}]	100	100	100	100	100	**100**
FOM [F/A. s]	431.0	44.01	553.4	317.5	561.8	**843.8**

The proposed buffer amplifier in this paper has an disputed performance in terms of the settling time which is the smallest value compared to many other previous proposed buffer amplifiers which are tested over a 1000pF capacitive load connected at the output. Even though the value of the quiescent current is about 3.95 µA, the overall FOM calculated value is 843.8 F/A.s which is the highest value compared to all previous studies from the literature, as summarized in Table II.

IV. Conclusion

In this paper, a high speed and high-performance rail-to-rail LCD buffer amplifier is proposed which has a very simple circuit structure. It consists of only 11 transistors in the core structure. DFVF input stage followed by a high gain stage is used with a classic class-AB output stage. The total gain of the gain stage is so high so that a very high valued feedback factor is obtained. This increase in the feedback factor allows obtaining very small output impedance and as a result the circuit becomes an ideal candidate to draw high valued capacitive loads. The buffer is simulated using the 0.35µm standard CMOS technology parameters. From the results, the settling time is found to be only 0.3 µs showing very good performance in terms of speed compared to many other previously buffer designs whereas the quiescent current is 3.95 µA. The circuit is also laid out using Microwind and the layout area is obtained as 2904 µm^2. Among the simulations, Monte Carlo analysis is also performed and as a result it is found that the buffer has a good robustness towards tolerance and other process mismatches. Also, a fair comparison is carried out using the defined FOM value and it is demonstrated that the presented buffer amplifier shows an excellent and much better performance compared to other presented works from the literature.

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