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Non-isolated high step-up DC/DC converters – An overview

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Gain cell

Abstract High step-up, high efficiency, low cost DC/DC converters have operated as an interface to make use of the renewable energy system generated power. In order to obtain desired output voltage, the DC/AC voltage conversion to AC mains voltage is an important consideration mainly achieved through inverters. Taking into acoount the performance of the non-isolated high step-up DC/DC converters for the renewable energy systems, the substantial amount of topologies studied in past years are the non-isolated high step-up DC/DC converters. Based on proposed and generalized configurations, the non-isolated high step-up DC/DC converters are classified into several categories and reviewed in this paper. So, to clarify the distinguishing solutions, the key features; topological variations, merits and demerits of these converters are discussed and compared. This review work aims to give a well-informed and a well-detailed general framework about these converters and facilitates to derive the new well topologies in the future.

Contents

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1. Introduction

Progressive decline of the conventional fossil fuels due to extensive usage has led to immense environmental issues and search for the important renewable energy sources like photovoltaic (PV) panels, fuel cells (FC) and wind power is getting more consideration [1,2]. The electric power of the renewable energy sources is delivered at the output voltage range of 12 VDC to 70 VDC [3]. In residential application for a promising and growing PV power systems, the output voltage of the PV power source needs to be increased in order to satisfy DC bus voltage for the inverters (380 V for the full bridge inverters and 760 V for the half bridge inverters). The PV series-connected configurations applied to upgrade the output voltage of the PV system decrease the power level of the system due to the module mismatch and shadow effect. As long as PV parallel-connected configurations deliver the electric power at low output voltage, the high step-up converters are required to upgrade this low voltage to high voltage [4–6]. The power source fuel cells used in the electrical vehicles and distributed power systems also need a high step-up converter to increase the low fuel cell output voltage to higher voltage [7,8]. Furthermore, high performance step-up converters are employed in a wide range of industrial applications such as in medical equipment, battery-discharged dc converter in UPS system, automobile HID headlamps [9,10].

In high step-up applications, conventional boost converter is not a convenient option due to its low conversion efficiency, which requires an extreme duty cycle. Many proposed techniques can be found in literature for the basic step-up converter to extend its voltage gain. The first section covers the utilization of basic step-up converters with switching inductor/capacitor cells which extend the voltage gain of the converter by increasing its inductive and capacitive energy. Various switching inductor/capacitor techniques like voltage lift, re-lift, self-lift as well as the active/passive switching inductor techniques are mentioned in this category. During one switching cycle, all the inductor/capacitor cells are charged in parallel and discharged in series [11–24]. The voltage multiplier cells based on the Cockcroft-Walton and Dickson voltage multiplier are widely used in this category [25–29]. Second kind is of cascaded converters in which quadratic cascade converters has a high voltage gain without extreme duty cycle [30–34]. A series boost converters with a high voltage gain and a low system efficiency can be integrated into one switch [35]. By associating these cascade converters with various switched inductor/capacitor cells, various cascade topologies named as the triple-lift, the high order lift, the super-lift and so on, can be accomplished with a rather higher voltage gain [36–41]. However, the conversion efficiency of these multistage cascaded converters is quite low due to the multistage power process. The third segment covered here is about stacked converters. There are various topological variations with a common input section, and common current source that are named as three level boost converters [42–48]. The power level of single switch high step-up converter is limited to power switch rating. So, the interleaved converter with voltage multiplier cell presented in the fourth portion raises both power rating and voltage gain of the converter [49–52].

Finally, the fifth category comprises of coupled inductor high step-up DC/DC converters. Non-isolated high step-up coupled inductor DC/DC converters are derived from circuit variations of the five basic step-up converter topologies; boost, buck-boost, cuk, zeta and sepic converters. The coupled inductor boost, sepic converters and their derived topologies have received more attention than the others. These converters provide a very high voltage gain with high sensitivity at duty cycle extremes [53–103,105–152]. The common feature of these converters lies in the increased utilization of the semiconductor devices at very low or high duty cycles, since voltage gain is adjusted by turn's ratio of the coupled inductor to avoid the extreme duty cycle. A coupled inductor approach to achieve a high voltage gain has some penalties. Many different topologies have been proposed to overcome the damages arising from leakage inductor, input current changes, big magnetic core volume, and so on.

An overview of the high step-up coupled inductor boost converter is presented in [137]. A high step-up voltage gain integrated DC/DC converters and their methodology synthesis and analysis are covered in [138,139]. The voltage multiplier cell concepts and their topological variations in the coupled inductor boost converters are covered in detail in [120]. The inner connections between the coupled inductor boost converter topologies, their component stress are clarified in [112] and [108].

In this paper, the associations of the basic step-up converter with the extension techniques of the voltage gain are systematically generalized and categorized by dividing the basic step-up converters into two or three sections and then merging these sections with related voltage gain techniques in the basic

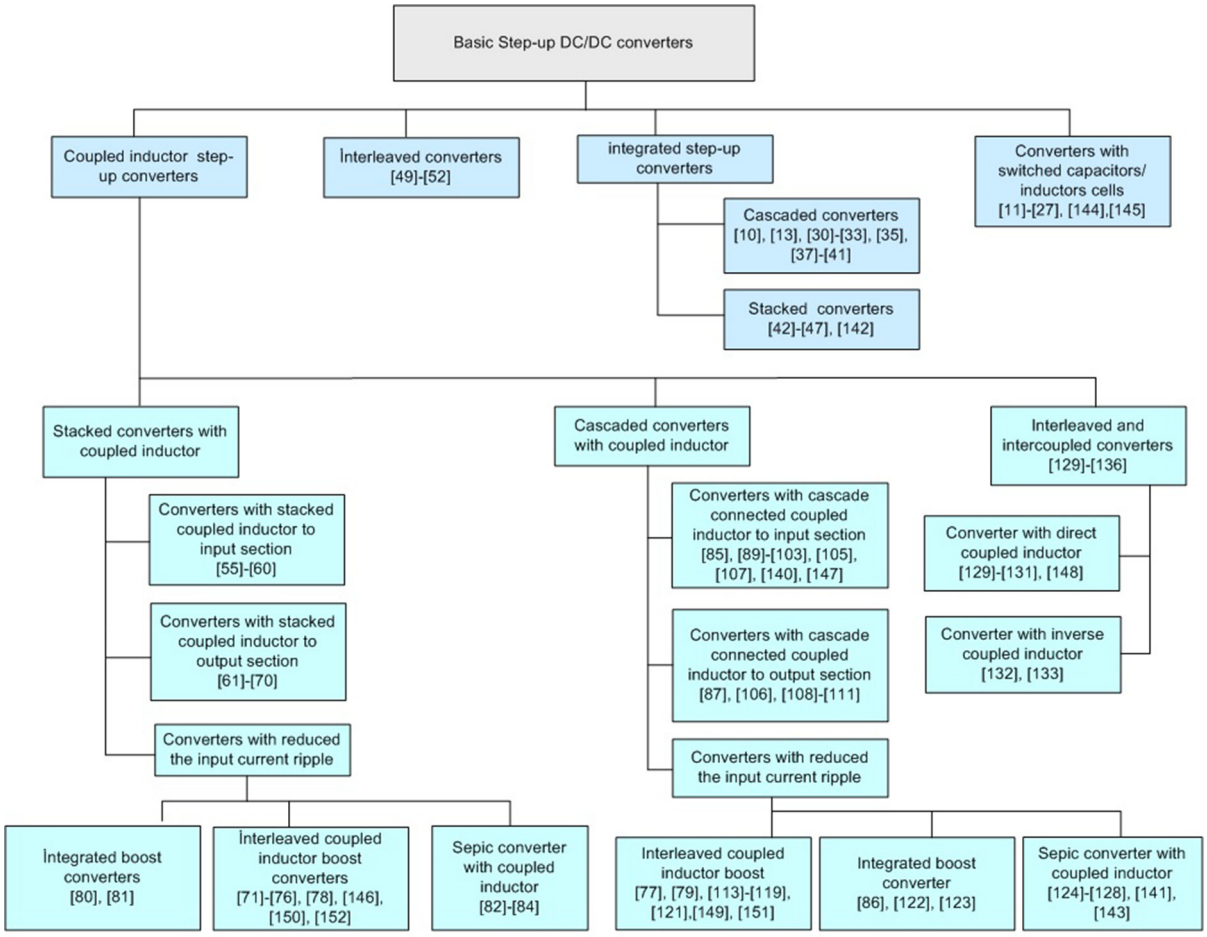

Fig. 1 Classification of non-isolated high step-up converters.

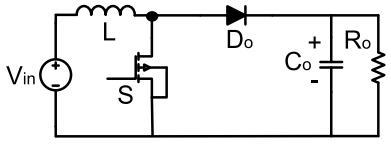

Fig. 2 Conventional boost converter.

step-up converters. Based on these generalizations and categorizations, the significant majority of the non-isolated high step-up DC/DC converters published in literature are comprehensively and comparatively reviewed. The evaluated non-isolated high step-up DC/DC converters are classified as shown in Fig. 1.

2. Basic step-up converter with switched inductor/capacitor cell

Boost converter; a basic step-up converter (Fig. 2) is widely employed in the step-up applications mainly due to its simple and efficient structure. Theoretically, while duty cycle is close to one, voltage gain of the boost converter is close to infinite. However, when switch turns-on period becomes longer, conduction losses are increased, turn off current ripple becomes high, and hard switching operation is a significant problem since the switching and reverse recovery losses become high. In high step-up applications, since voltage stress on power devices are equal to the output voltage of the converter, a high voltage rating power switch with high $R_{DS\text{-}ON}$ leads to increase conduction losses and cost of the converter. So, the voltage gain of the conventional boost converter is limited due to the low system efficiency.

In [36], a series of topological constrains is introduced in DC/DC converter to clarify the roles of inductors and capacitor in various converters as current and voltage elements respectively. The use of various switched inductor and/or capacitor cell to enhance the voltage gain is justified. Capacitors and inductors employed as a buffer neither generate nor consume any power. These current and voltage elements absorb and store energy from the input section at one moment and transfer it to another output section at another [36]. Therefore, the capacitors are utilized as voltage source in input section, voltage buffer in the middle section, and voltage load in the output section of the basic six DC/DC converters. These can be replaced by various switched capacitor cells to increase capacitive energy storage/transfer mechanism, thus resulting in an enhanced voltage gain. Similarly, the inductors placed as current source in input section and current buffer in middle section of the these converters can be replaced by switched inductor cell or switched inductor and capacitors cell to boost magnetic energy storage/transfer mechanism, thus resulting in a higher voltage gain (vide Fig. 3).

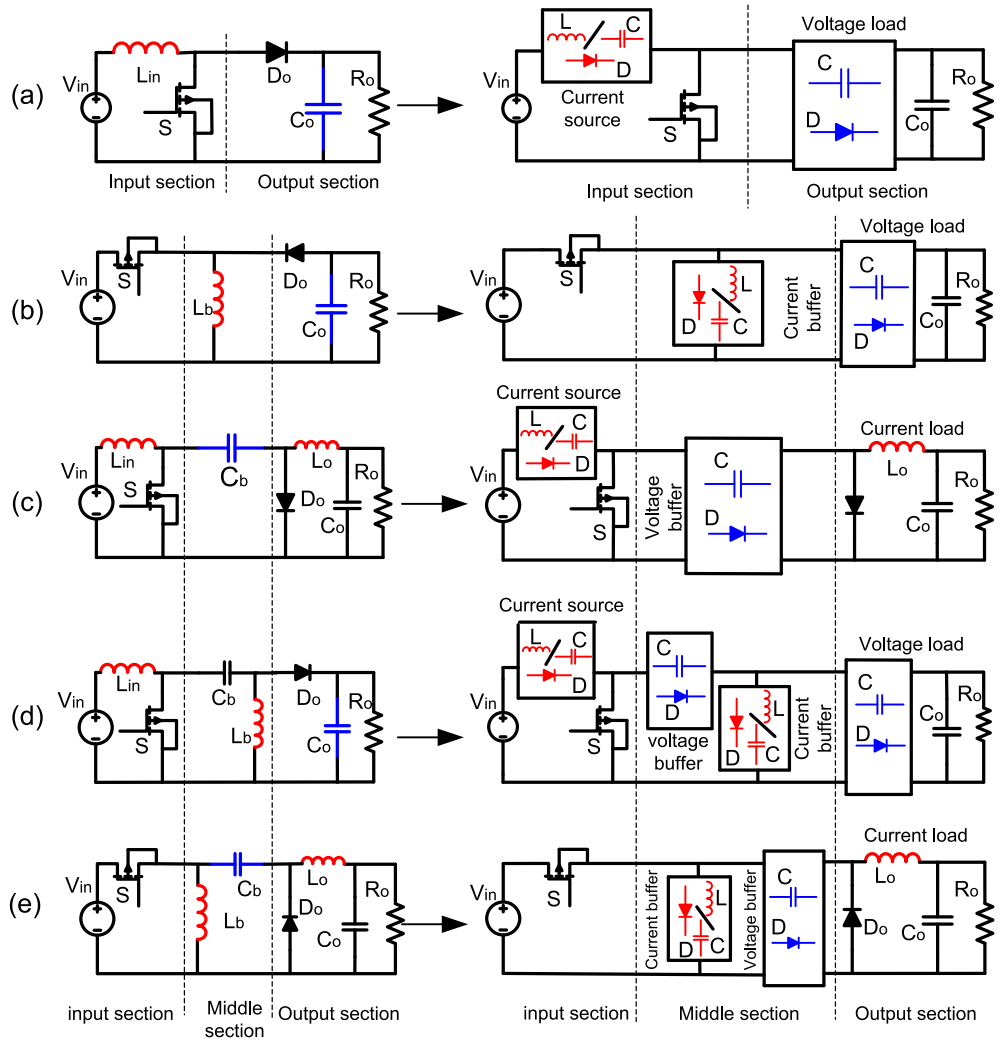

Fig. 3 General configuration with switched inductor/capacitor cell of (a) boost converter, (b) buck-boost converter, (c) cuk converter, (d) sepic converter, (e) zeta converter.

Voltage and current elements demonstrated in Fig. 4 and Fig. 5 respectively can be adopted to upgrade voltage gain of the basic step-up converter. In all switched inductors/capacitors in Fig. 4, as V_{ab} becomes positive, all parallel connected energy storage components are charged, and as V_{ab} becomes negative, all are series connected and discharged. Some extended types of these current elements are illustrated in Fig. 4d and Fig. 4e.

In all switched capacitors depicted in Fig. 5, S as main switch is turned-off, all capacitors are parallel connected and charged, and when the main switch S is turned-on, all of the capacitors are series connected and discharged. Also, voltage multiplier cells as voltage elements presented in Fig. 6 can be used up to upgrade the obtained gain (Fig. 6c) [25–27].

One or more of the switched inductor/capacitor and switched capacitor cells shown in Fig. 4 and in Fig. 5, respectively can be applied on their related place in the basic step-up converters to increase voltage conversion ratio without extreme duty cycle as shown in Fig. 3. As long as these voltage elements are used by series-connected to input section of the basic step-up converters, voltage stress on the active switch and output diode are decreased. Switched capacitor cells, in which if a switch is connected between dot A and dot B (Fig. 5a), becomes similar to that of in Fig. 5b as long as these switches are employed as main switch of the converter. The extended type of these switched capacitor cells in Fig. 5a and Fig. 5b is introduced in [144]. Switched capacitors in Fig. 5 have identical functions except for that in Fig. 5d. As different from these switched capacitor, the active–passive switched capacitor cell in Fig. 5d can also be used to extend input voltage. Some proposed converters employing these voltage and current elements are depicted in Fig. 6.

Another switched inductor topology as active switched inductor cell is shown in Fig. 7. This introduced to converters with current source a high voltage gain, distributed voltage stress on the switches, low current stress through the switches, and an easy control with applying same control signal on the switches. However, with this active switched inductor topology, voltage stress on the output diodes becomes higher than output voltage. Voltage conversion ratio can be increased by replacing the inductors in this active switched cell with one of the current element cells which was demonstrated in Fig. 4 to the design shown in Fig. 8. All inductors in these active/passive switched inductor cells are charged in parallel

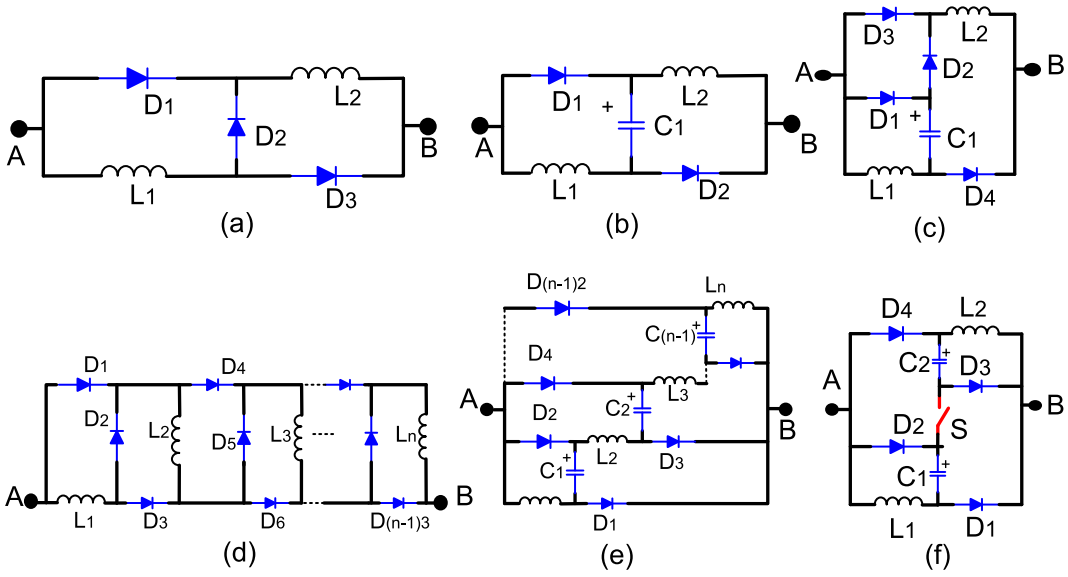

Fig. 4 Switched inductor/capacitor cells representing thecurrent element, (a) topology presented in [11], (b) topology presented in [20] and [145], (c) topology presented in [19], (d) extended cell of [5] presented in [41], (e) extended cell of [11] presented in [21], (f) topology presented in [19].

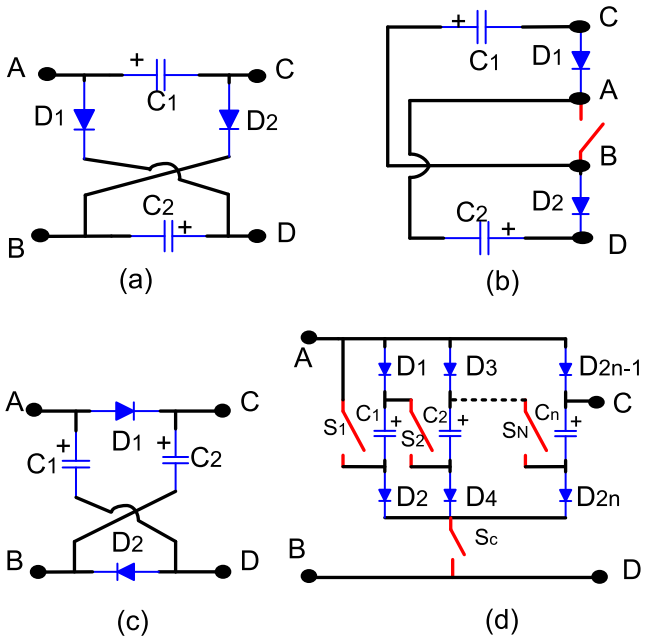

Fig. 5 Switched capacitor cells representing the voltage element, (a) topology presented in [11], (b) topology presented in [14], (c) topology presented in [11], (d) topology presented in [12].

by the voltage source while the same turn-on signal is applied to active switches. The stored energy in these inductor is transferred in series to output section as the same turn-off signal is applied to active switches.

In the converter with symmetrical topology in Fig. 8b, switches have same voltage stress. If different value inductor is employed in this converter, maximum voltage stress across the switches and diodes is increased. With the asymmetrical topology in Fig. 8a, component count is decreased, thus decreasing the voltage gain and increases the maximum voltage stress on the active switches. By using voltage multiplier cell based Cockcross Watson multiplier at the output section of the converter in Fig. 8c, voltage conversion ratio is even more raised [23,24].

The major flaw of high step-up converters with switched inductors/capacitors cells is hard switching operation. Another big issue is the increasing number of converter's devices for much higher voltage gain. This leads to an increased volume, cost, loss of converters and restricted power level raise. By increasing the number of switched capacitors/inductors, the pulsating current of capacitors and inductors' current flowed through switches and/or diodes during the charging of capacitors and inductors has also increased. This current stress leads to an increased switching and conduction losses. While considering the ESR resistances of the capacitor and conductor resistance of the inductor which are connected in series during power flow from input to output, power dissipations of converter is increased.

3. Cascaded step-up converters

The cascaded boost converters shown in Fig. 9 have a quadratic feature. So, these topologies with the simple and compact structure for a high and effective voltage gain is competitive candidates. To achieve a higher voltage gain, cascade boost converter in Fig. 9b can be extended as shown in Fig. 10. The difference between the two extended converters in Fig. 10 is voltage/current stresses on the diodes in m series. In Fig. 9a, semiconductor devices in first boost stage of cascade boost converter has less voltage stress than semiconductor devices in the second boost stage. A low voltage-rated switch has a low $R_{DS\text{-}ON}$ and this significates a low conduction loss. Low voltage stress on the power switch reduces switching losses and EMI noise. Therefore, in same operation frequency of switch S_1 and S_2, switching losses of switch S_1 is less than

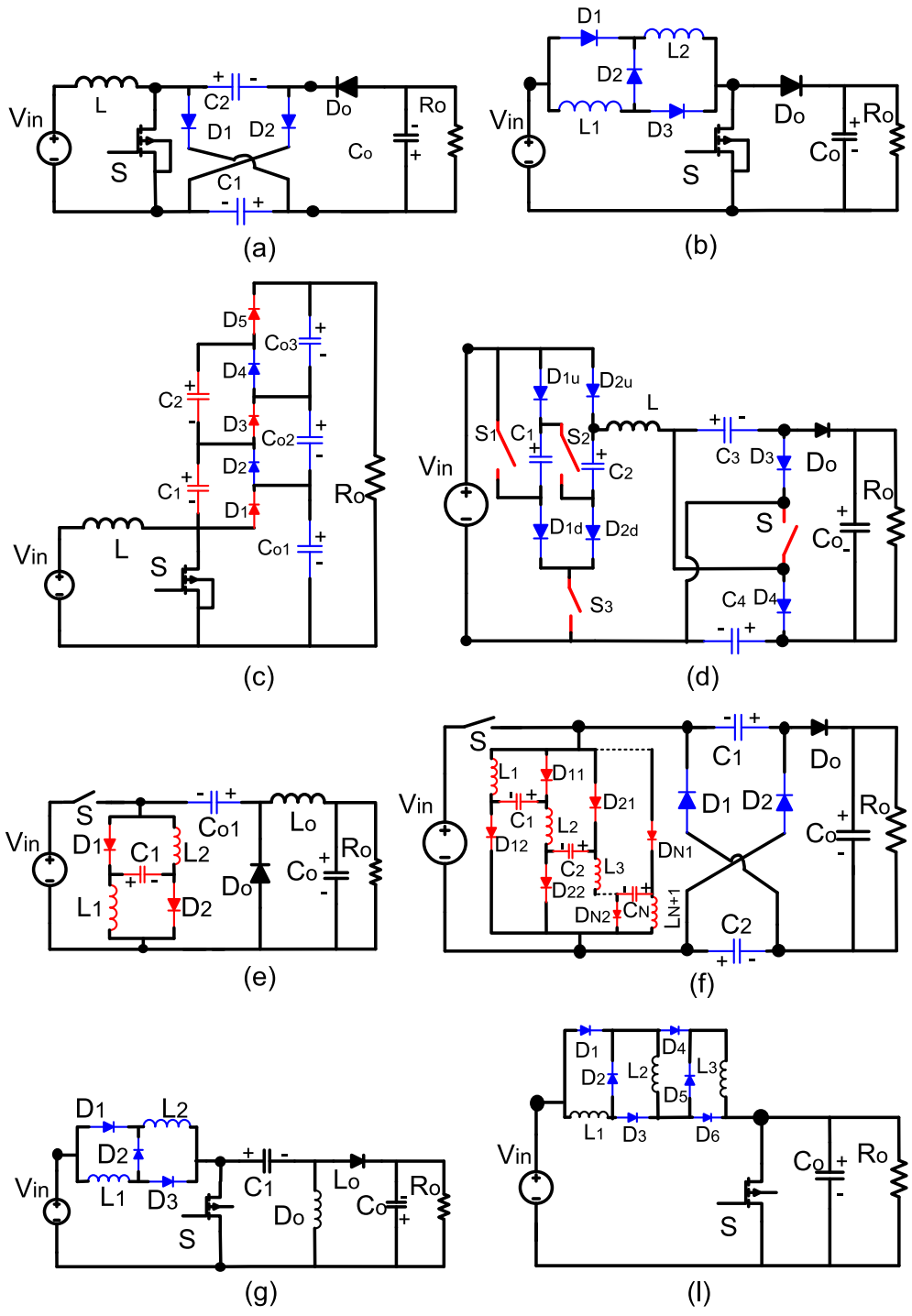

Fig. 6 Derivation of the basic step-up converters with improved current and voltage element cell. (a) Topology presented in [13], (b) presented in [11], (c) boost converter in [25], (d) presented in [15], (e) presented in [20], (f) presented in [21], (g) presented in [11], (l) presented in [41].

that of switch S_2. This allows an enlarged system's efficiency and power density for the first boost. However, the converter in Fig. 9a has two power switches that leads to more switching losses, cost and volume of the converter, difficulty of realization of soft switching methods for semiconductor devices and control circuit. Also, due to the stability problem of cascade boost converter in Fig. 9a, difficulty of control system's design increases. With the topologies in Fig. 9c and Fig. 9d voltage stress on the buffer capacitor C_1 is reduced.

The converter's composition in Fig. 11a, boost and sepic converters are integrated into one switch. Thus, this cascade converter has quadratic aspect same like those of in Fig. 9. Current element L_{in} of the converter in Fig. 10b can be replaced with switched inductor/capacitor cells consisting of

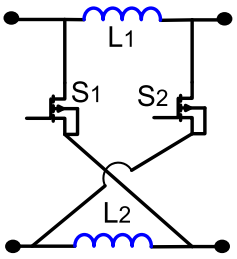

Fig. 7 Active switched inductor cell [34]

L_{in}, D_{in}, C_{in} and likewise, currents elements L_1, L_2, …, L_n respectively in a series of the Fig. 10b converter, can be replaced with switched inductor/capacitor cells consisting of L_1, D_1, C_1; L_2, D_2, C_2; …; L_N, D_N, C_N in a series (vide Fig. 11c). Thus, current and voltage elements in these cascaded converters and their extended types can also be replaced with switched inductor/capacitor cell in Fig. 4 and Fig. 5, respectively, to upgrade obtained gain as shown in Fig. 11

Voltage stress on the output diode and switch of these cascaded boost converters used in the high voltage application are significantly high. Thus high rated voltage of power devices leads to increased conduction losses. By extending these cascaded boost converters like in Fig. 10, power process stages have enlarged throughout from input section to output section of the converter that decreases the system's efficiency. The increasing voltage stress across power switches increases switching losses, which is alleviated by applying ZVT in converter in Fig. 9e. In this active soft switching cell, resonant energy stored in resonant inductor L_r at first quarter of the resonance period is released to output of the converter by resonant capacitor C_r in which the resonant energy is stored at the second quarter of the resonance period. By this soft switching cell, Zero Voltage Transition (ZVT) and Zero Voltage Switching (ZVS) turned off for main switch, and Zero Current Switching (ZCS) turned off and ZVS turned on for the output diode are realized.

4. Stacked basic step-up converters

The five basic yet different converter topologies are; step-up converters: boost converter; buck/boost and its duality, cuk converter; sepic converter and its duality and zeta converter. As mentioned in section-II, these converters are introduced as a planar, ladder-like structures in [36] and comprise of two or three sections. The boost converter consists of the input section (voltage source or current source) and the output section (voltage load or current load). The other addition to these sections comprises of a middle section (current buffer and/or voltage buffer). Common current sources or common current buffer can be used as an integration part of two or more basic DC/DC converters (vide Fig. 12). However, only common current sources adopted as an integration part can be performed to enhance the converter voltage gain by stacked association of some of the basic converters. These integrated converters with the stacked output are mentioned in Fig. 12b.

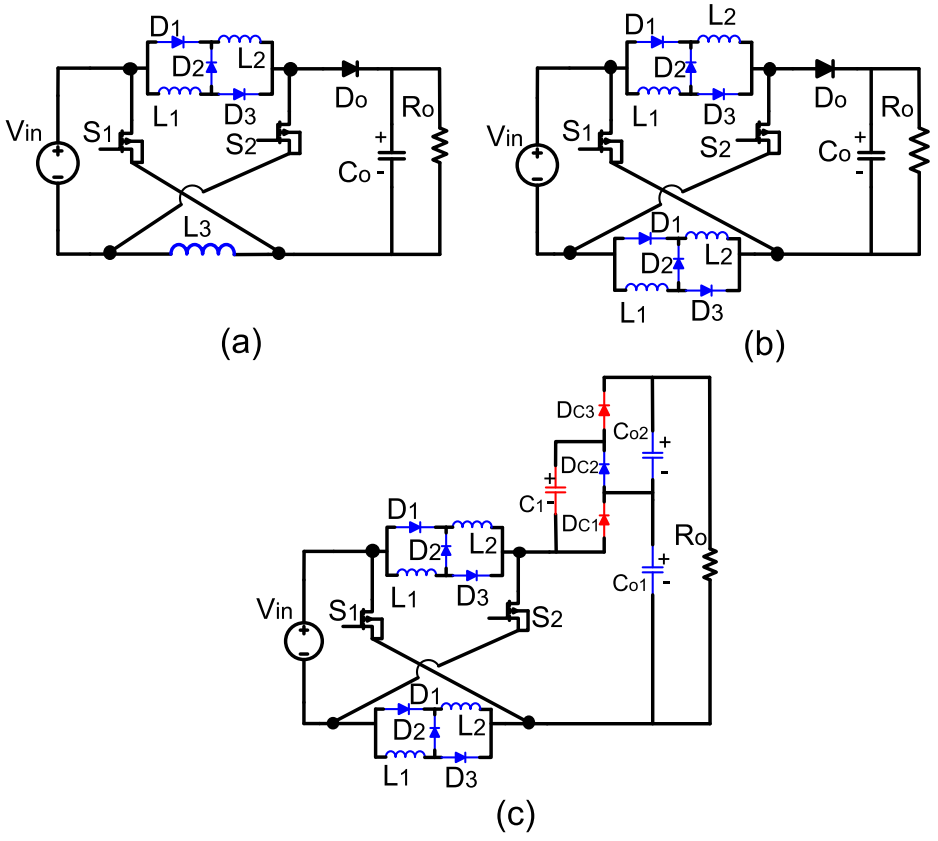

Fig. 8 The converters with active/passive switched inductor. (a), (b) Topologies presented in [22]. (c) Topology presented in [23].

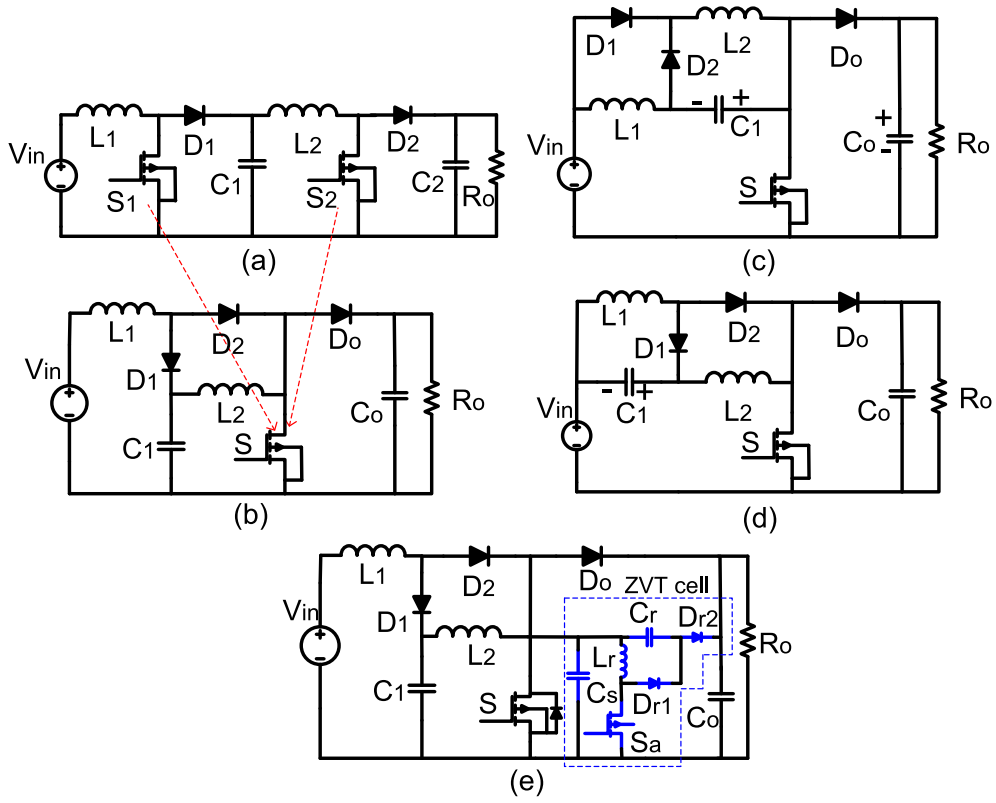

Fig. 9 Cascaded converters, (a) topology presented in [30], (b) topology presented in [33], (c) topology presented in [31], (d) topology presented in [32], (e) topology presented in [10].

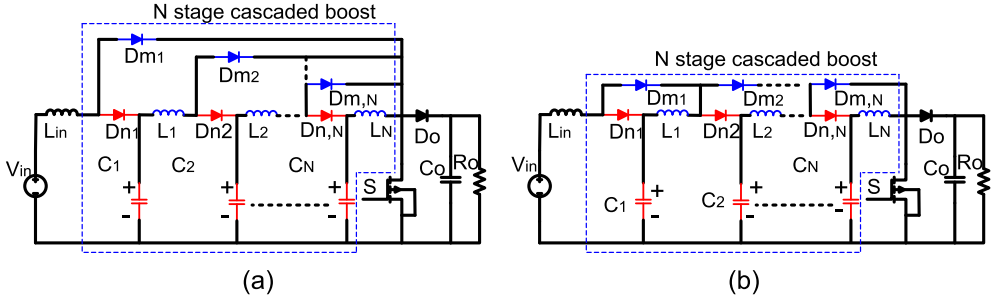

Fig. 10 Extended cascade boost converters, (a) topology presented in [35], (b) derived topology from in [30].

These planar, ladder-like structures and their duality ensure the basic converter that their association with stacking output of the converters will improve the voltage gain. Sepic converter and its duality, zeta converter, can be integrated as displayed in Fig. 13b. While, cuk converter and its duality, buck-boost converters, can be integrated as represented in Fig. 13c, and finally boost and zeta converters can be integrated as shown in Fig. 13a. An example for the stacked converters is given in [142] in which self-lift-sepic converter and cuk converter has a similiar input section.

Another stacked type converter shown in Fig. 14 is a three level boost converter. The voltage conversion ratio here is double to that of the conventional boost converter due to the two boost converter with a common current source are stacked with two main switches and output sections. With this topology containing two main switches, voltage stress on the main switch is reduced to half of the conventional boost converter. This distrubuted voltage stress results in employing a high performance power switch with low $R_{DS\text{-}ON}$ to decrease the cost and conduction losses of the converter and an operation under high voltage and high frequency conditions. However, the converter in Fig. 14a has a hard-switching performance. Many soft switching cells are required for these two main switches.

Two passive snubber cells in converter of Fig. 14b realize a soft-switching performance for main switches S_1 and S_2, and to alleviate reverse recovery problem of the output diodes, D_{o1} and D_{o2}. Each soft switching cell consists of the resonant capacitor $C_{r1(2)}$, storage capacitor $C_{s1(2)}$, resonant inductor $L_{r1(2)}$ and diodes D_{11}, D_{12}, D_{13}, D_{21}, D_{22}, D_{23}. In the steady state processes of this three level converter with passive loss-free snubber cells, at first resonant stage, ZCS turn on and ZCS turn off are realized for switches $S_{1(2)}$ and $D_{o1(2)}$, respec-

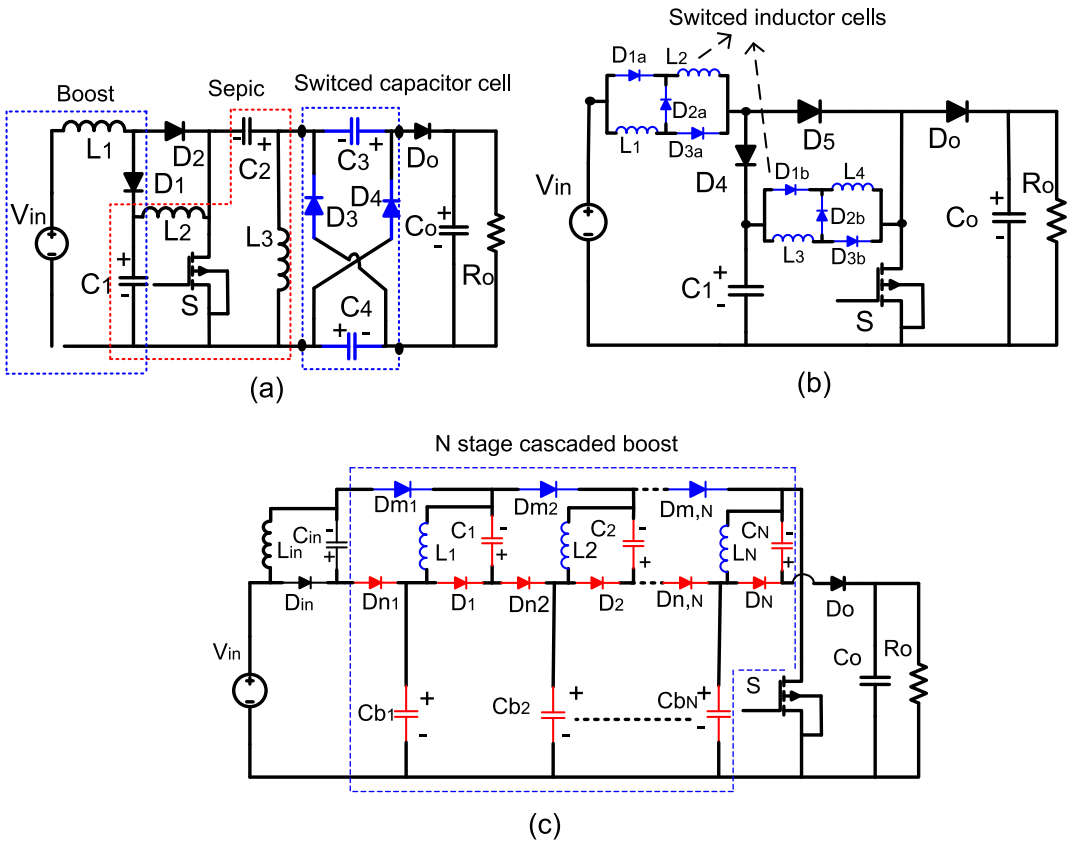

Fig. 11 Cascaded converters with switched inductor/capacitor cell, (a) topology presented in [36], (b) topology presented in [40], (c) topology presented in [37].

tively, by resonance inductor $L_{r1(2)}$ and at the end of this stage, resonant energy of the inductor $L_{r1(2)}$ is stored at storage capacitor $C_{s1(2)}$. At next resonant stage, ZVS turn off and ZVS turn on is observed for $S_{1(2)}$ and $D_{o1(2)}$, respectively, by rezonant capacitor $C_{r1(2)}$ and at the end of this process, stored resonant energy in capacitor $C_{s1(2)}$ is released to output of the converter. However, current stress through main switches $S_{1(2)}$ and voltage stress across output diodes $D_{1(2)}$ is increased by passive snubber cell.

While comparing the stacked converters and cascade converters, voltage gain and efficiency of converters in the ordinary cascade structure are equal to the multiplying of output voltage gains of the each converter to the efficiency of the each converter, respectively. Although the voltage gain increases this way but the system efficiency is reduced, as long as the power flowed from the input to output is processed twice. Voltage gain and efficiency in stacked converters is equal to the sum and average of each stacked converters, respectively. Even though voltage gain is inherently less for cascade than its counterpart, efficiency of stacked converters is higher than that of the cascade converter, as long as the power is shared with each cell of the stacked converters.

5. Interleaved boost converters with voltage multiplier cell

Interleaved boost converter is widely used in Power Factor Correction (PFC) applications. The limitations of conventional boost converter at high power applications such as high current ripple, increased reverse recovery losses, heightened passive component size, reduced power density, and delayed transient response time encourages the use of interleaved boost converter over conventional boost converter. However, for high step-up applications, the conventional boost converter's problem of increased voltage stress and current ripple of power devices in short switching-off period is also observed in conventional interleaved boost converter. Converters proposed in [49–52] (Fig. 16) achieve high voltage gain without extreme duty cycle by using voltage multiplier cells integrated in conventional interleaved boost converter. Yet, hard switching operation of power switches in these converter is still a big problem.

Literature shows that voltage multipliers (see Fig. 15) are widely adopted in high step-up converters to upgrade voltage gain. As shown in Fig. 16, these voltage multiplier cells are also used in conventional interleaved boost converter. Voltage multiplier cells in Fig. 15c and Fig. 15d can be derived from Dickson and Cockcross-Walton multiplier. By using loop I in Fig. 15a, a constant voltage across capacitor C_2 placed between m_1 and m_2 in Fig. 15c is achieved, and likewise, by using loop II in circuit in Fig. 15a, a constant voltage across capacitor C_4 in Fig. 15c is achieved. In similar way, the circuits in Fig. 15c and Fig. 15b can be also associated. Eventually, resultant circuit shown in Fig. 15d is obtained by replacing the anodes' connection dots of diodes D_2, D_4 and D_6 in Fig. 15b.

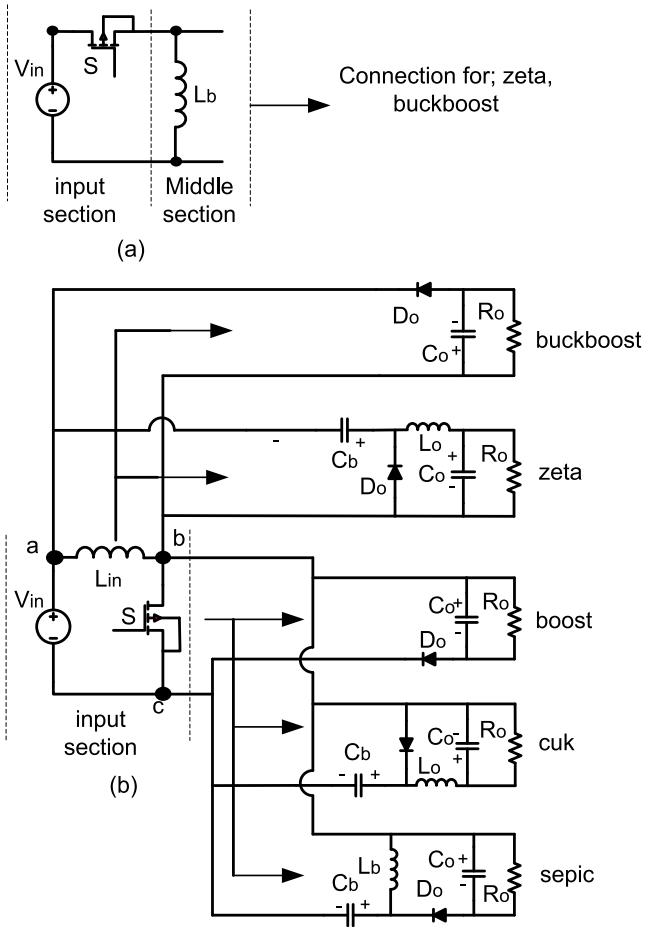

Fig. 12 (a) Voltage type input section and common buffer section, (b) circuit diagram of common current source and its correspondent middle and output sections.

Since switches in the interleaved converter is driven at the different phases, voltage between output terminals of interleaved converters A and B contains a square wave from $V_{in}/(1-D)$ to $(-V_{in}/(1-D))$. Therefore, voltage multiplier cells are applied between dot A and dot B to extend the gain obtained. However, switching losses and conduction losses are increased because of the additional current flowed through the switch by charging the capacitor of the voltage multiplier cell. As long as the current balance between the branches of interleaved boost converters is not achieved, the power level raise of converter will be limited due to the higher load on one branch.

By interleaving the cascade converter in Fig. 9b and adding a voltage multiplier cell, the converters in Fig. 16c and Fig. 16d are derived. The topologies in Fig. 16 with voltage multiplier cell highlight these features; a low voltage stress on the switches and output diodes, a low input current ripple which is suitable for high power application due to the shared current stress and input power between individual boost converters. While assuming V_x as voltage stress on the switches in switch-off time, the effect of voltage multipliers on the voltage gains of these converters in Fig. 16 are similar except for voltage multiplier in Fig. 16a and Fig. 16e. Thus, the topology with lesser components shown in Fig. 16d can present similar voltage gain with the converter in Fig. 16c. A modified Dickson voltage multiplier in Fig. 16e is connected between terminals A and B to obtain a high voltage gain. The voltage multiplier cell used in the converter in Fig. 16a has a symmetry and doesn't impact modular structure of the interleaved boost converter, hence it can be extended easily. But others are not modular as duty cycles of the switches should be overlapping in these converters. So, same duty cycles operating at 180° out of from each other should be greater than 0.5. Improvement in voltage gain of the converter in Fig. 16a is low when compared with others.

Performance comparison of the converters with noncoupled inductor chosen from section 1–5 is demonstrated in Table B in appendices.

6. Coupled inductor step-up converters

The layout of the inductor and/or capacitor in the middle section of basic converters resembles the high pass LC filter [36]. This feature is especially obvious in zeta and sepic converters. This unique feature implies to converters so that ac power pulses can be flowed without hinder from the input to output section. Contrarily, the input–output section of this topological arrangement in basic converters is always in form of low-pass filter. In this regard, one can say that high frequency coupled inductor used in the middle section are more advantageous than the one used in input section. With the replacement of buffer inductor in middle section or the input inductor in input section with coupled inductor, secondary side of coupled inductors with N turn ratio employed as a flyback in all basic step–up converters contributes to converter a same voltage gain as ND/(1-D) in both their stacked and cascaded topologies [138]. Nevertheless, the boost and sepic converters with coupled inductor and their derived topologies have received more attention than others due to following advantages.

For boost converter with coupled inductor:

(1) a high conversion ratio with low component count is achieved;
(2) some proposed coupled inductor networks such as active switched coupled inductor network and coupled-inductor-inverse-network are introduced in input section of converter;
(3) a low input current ripple and quadratic feature are obtained by integrating boost converter into one switch.

For sepic converter with coupled inductor:

(1) high frequency coupled inductor can be used by replacing inductor in the middle section that is in form of high-pass filter;
(2) a low input current ripple can be inherently achieved without integrating an extra converter with current source;
(3) as secondary winding of coupled inductor is cascade connected to input section, gain obtained is enhanced as the gain of conventional boost converter with coupled inductor.

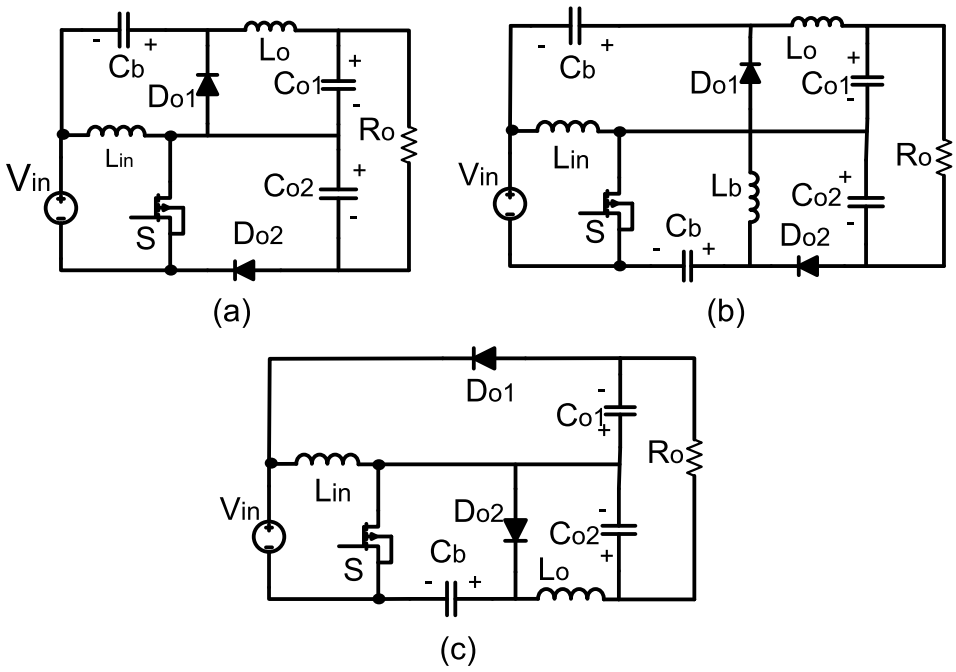

Fig. 13 Stacked topologies presented in [139] (a) by integrated boost and zeta converters, (b) by integrated sepic and zeta converters, (c) by integrated cuk and buck-boost converters.

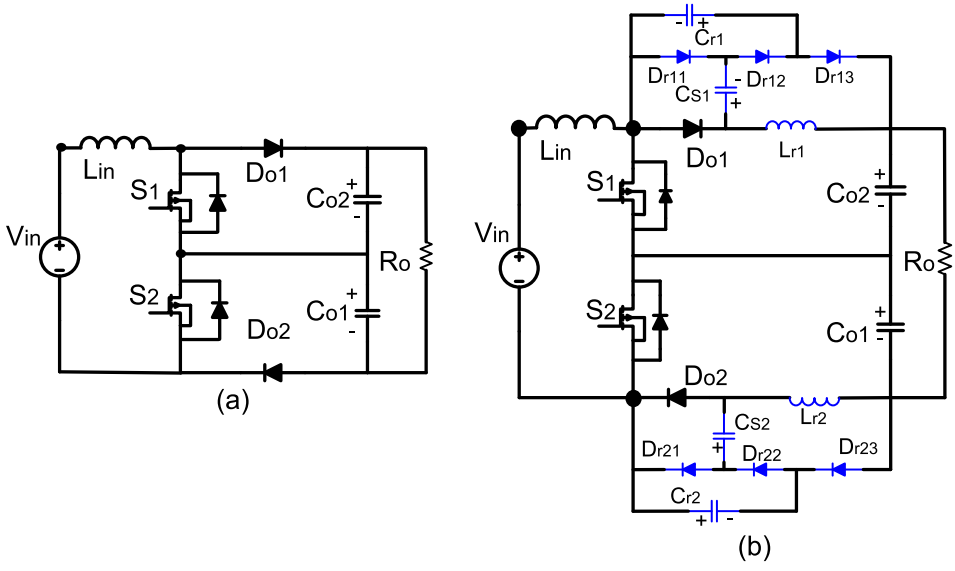

Fig. 14 Three level boost converter (a) presented in [44], (b) applied soft switching cells in [46].

Basically, secondary winding of coupled inductor for boost converter in [137] is introduced in form of cascade or stacked variant connections (see Fig. 17c). The configurations can be extended by associating these two connection with input section or output section of the boost converter. Similarly, these extended configurations can be applied for sepic converter. The details of these derived configurations are covered in later section of this paper.

Advantages of the coupled inductor for boost and sepic converters depicted in Fig. 17 are presented below:

(1) the contribution of the coupled inductor with N turns ratio in Fig. 17 to voltage gain of these converters is similar to ND/(1-D);
(2) the efficient usage of stored energy in magnetic core improves the utilization of magnetic core, resulting in a high voltage gain;
(3) the reverse recovery problem of output diode can be alleviated by leakage inductor;
(4) voltage stress on power switch are reduced and voltage gain can be adjusted by avoiding extreme duty cycle.

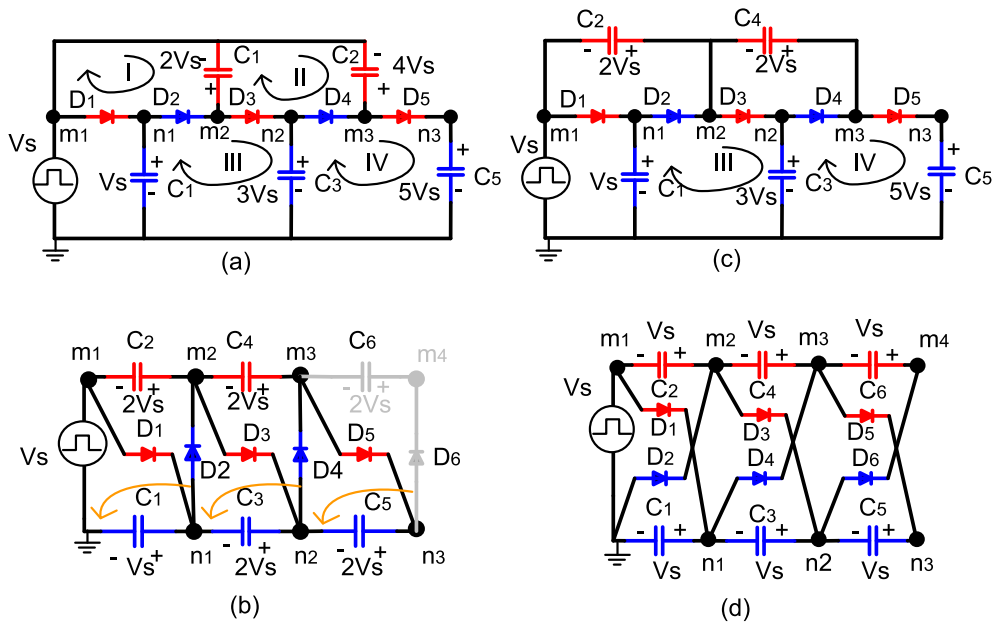

Fig. 15 (a) Dickson multiplier [29], (b) Cockcross-Walton multiplier [28], (c) topology presented in [51], (d) topology presented in [49].

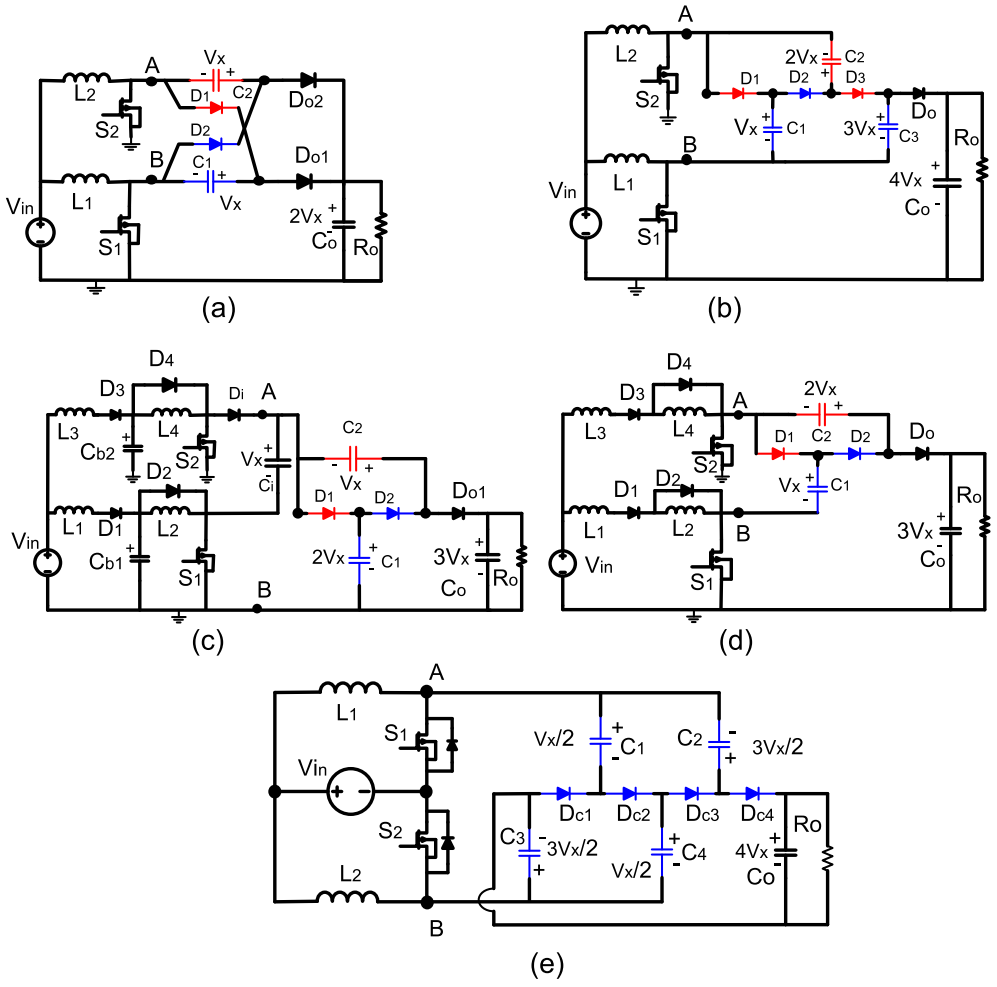

Fig. 16 (a) Converter in [49], (b) converter in [50], (c) converter in [51], (d) derived converter by using voltage multiplier in Fig. 6c, (e) converter in [52].

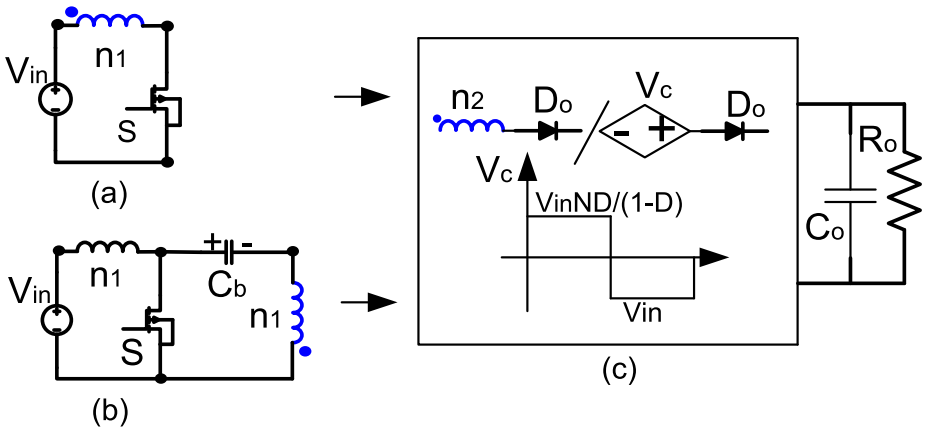

Fig. 17 The common use of the coupled inductor (a) in the boost converter, (b) in the sepic converter, (c) secondary side of the coupled inductor and its equivalent.

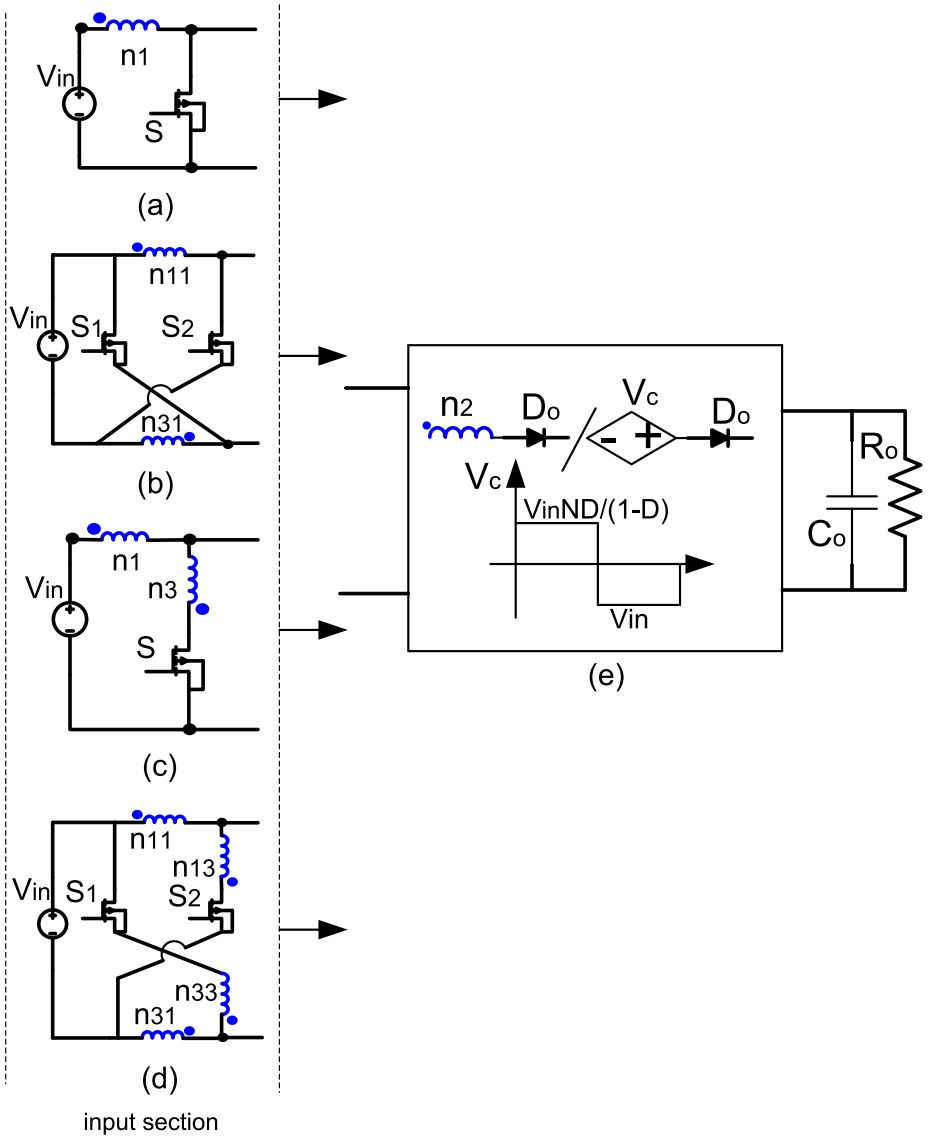

Fig. 18 (a) Input section of the boost converter with coupled inductor and (b) its active switched coupled inductor network. (c) Coupled inductor inverse network and (d) its active switched coupled inductor network. (e) Secondary side of the coupled inductor and its equivalent.

Following are the disadvantages of the coupled inductor for converters in Fig. 17:

(1) as turns ratio of coupled inductors increases, the magnetic core volume and leakage inductor also increases causing voltage spikes on the power switches and diodes thus increases dynamic operation range and control challenges of converter;
(2) the increase in turns ratio increases voltage stress on the output diodes;
(3) the input current ripple for boost converter is high. This leads to increase the EMI problems, a high RMS input current component results in conduction losses, effects life span of the renewable energy devices, increases the switch current stress and the use of the electrolytic capacitor in renewable energy system. When the turns ratios is increased, input current ripple become higher and the problems following this current ripple becomes more severe.
(4) As long as the coupled inductor are employed only as a flyback in these converter, storage energy in the magnetic core is delivered from primary winding of the coupled inductor to secondary winding while switch is turned-off and storage energy in the magnetic core is high. Hence, requiring big magnetic core.

In literature, the proposed various input sections with coupled inductor for particularly coupled inductor boost converter are depicted in Fig. 18. These two windings-one switches, two windings-two switches and four windings-two switches used in the input sections with coupled inductor present to converter various merits. However magnetic core size and leakage inductor of the coupled inductor are increased. Furthermore, above mentioned advantages and disadvantages for the coupled inductor are also valid for these topologies.

(1) One of the converters' family with coupled inductor (Fig. 18b) is derived from the active switched inductor, shown in Fig. 7 [34]. Since the inductors in this active cell are charged during switches turn-on state and discharged during switches turn-off state simultaneously by applying the same control signals on switches, these inductors can be integrated into one magnetic component. Therefore, active switched coupled inductor network of input section shown in Fig. 18a is depicted in

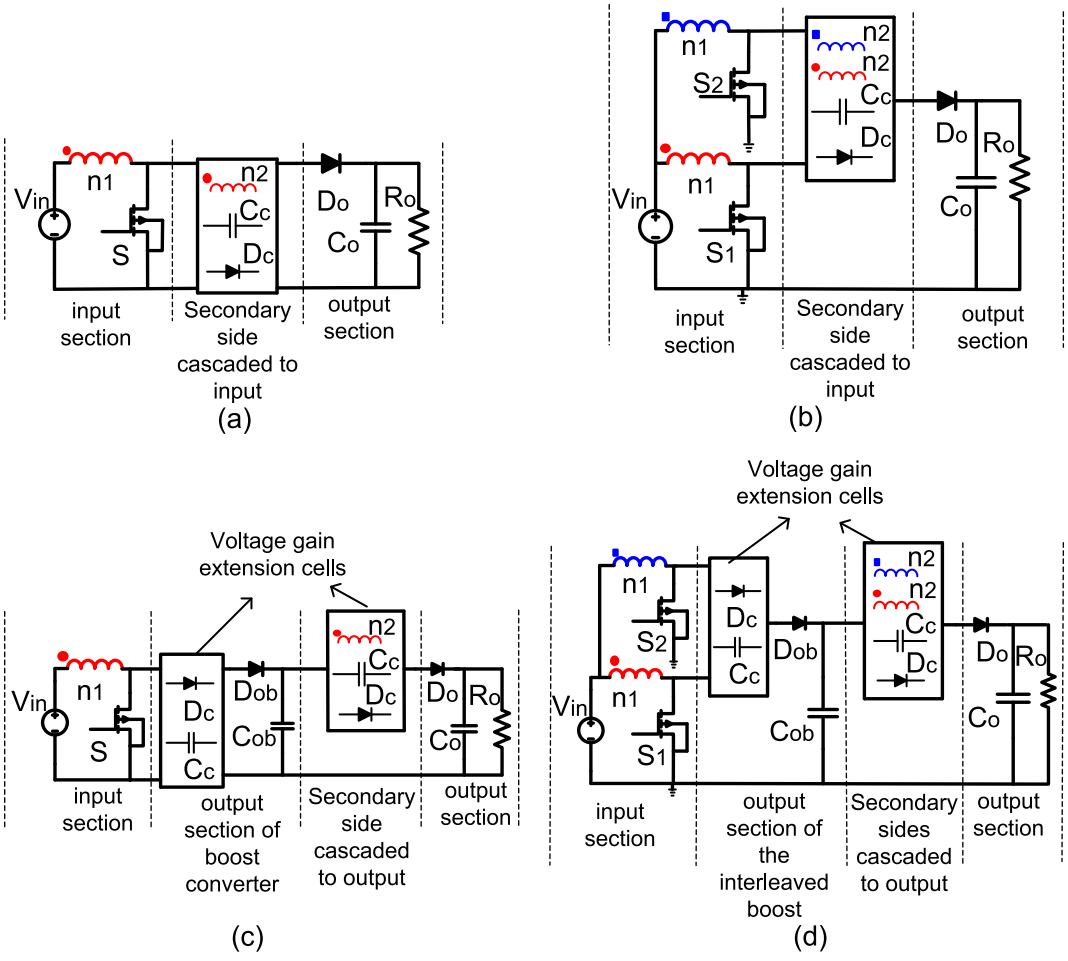

Fig. 19 General configurations of the cascaded coupled inductor boost converter. (a) Boost converter with cascade connected coupled inductor to input section and (b) its interleaved structure. (c) Boost converter with cascade connected coupled inductor to output section and (d) its interleaved structure.

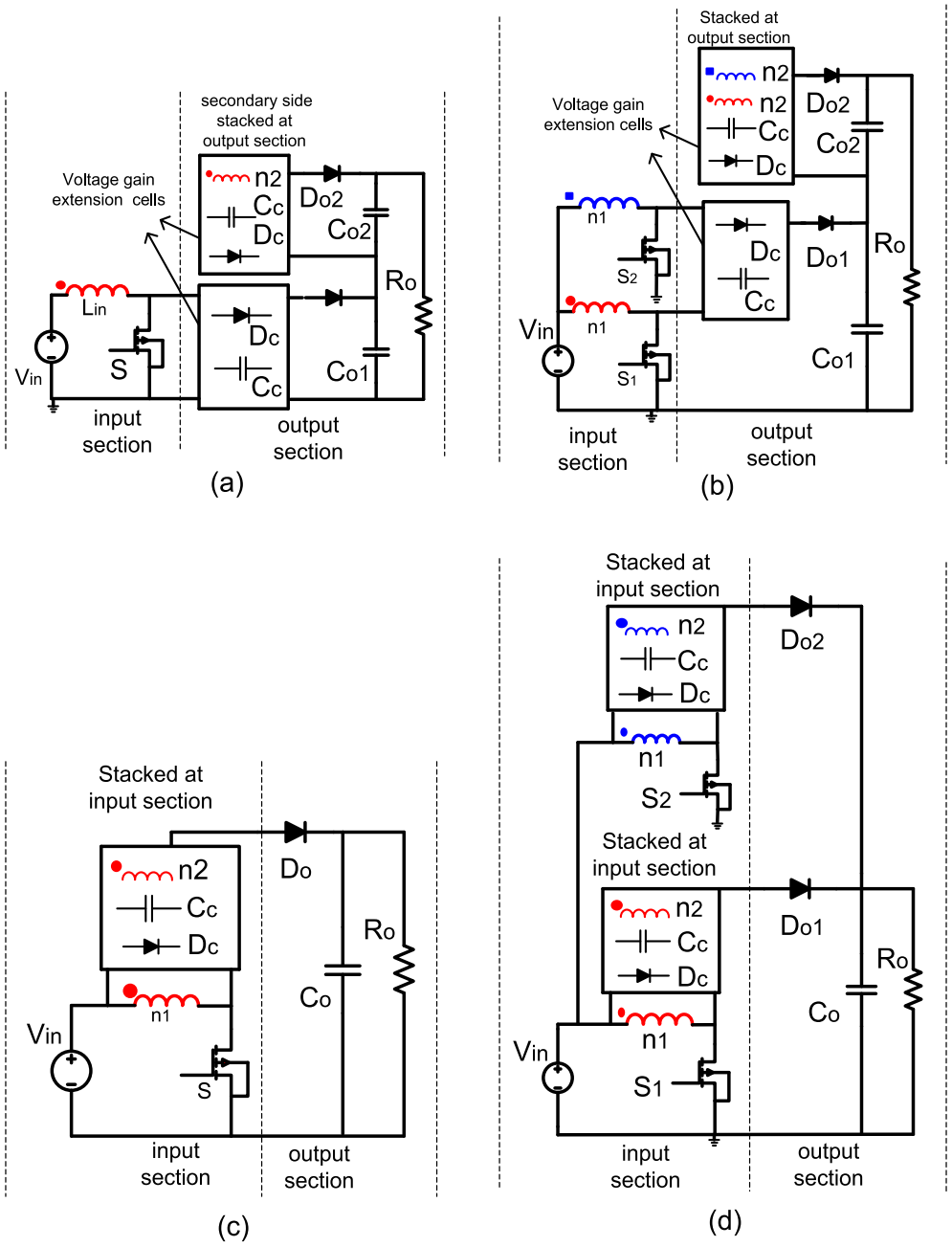

Fig. 20 General configurations of the stacked coupled inductor boost converter. (a) Boost converter with stacked coupled inductor at input section and (b) its interleaved structure. (c) Boost converter with stacked coupled inductor at output section and (d) its interleaved structure.

Fig. 18b. This topology improves the gain obtained and the utilization of the magnetic core, distributes the voltage/current stress on the power switches, and increases power density. However, this proposed topology for the input section also increases the voltage stress on the output diode.

(2) Another coupled inductor proposed for input section, shown in Fig. 18c, is named as coupled-inductor-inverse-network due to an inverse coupled windings in the input section, and its active switched coupled inductor network is depicted in Fig. 18d. With this topology, primary and secondary windings of the coupled inductor without multiplier cell contribute to voltage gain as N1D/[(1-D)(N1-N3)] and N2D/[(1-D)(N1-N3)], respectively. Thus enhances the utilization of the magnetic core. However, this inverse tertiary windings N3 contributes to voltage stress on the output diode as N3Vin/(N1-N3).

To overcome the above drawbacks of the high step-up converter with coupled inductor, many topologies have been proposed. The general configurations for improved topologies are derived below which are categorized into cascaded and stacked connection type of the coupled inductor that separately consti-

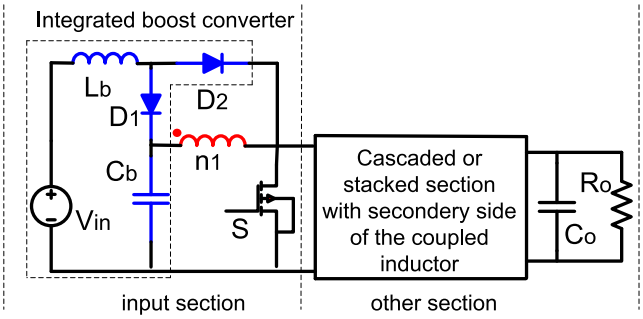

Fig. 21 General configuration of the coupled inductor boost converter being integrated with boost converter.

tutes for each sections of the boost and sepic converters. In general configurations of the coupled inductor boost converter, input section of converter can be replaced with any one of the mentioned input sections.

General configurations of boost converter with coupled inductor are demonstrated in Fig. 19, Fig. 20, and Fig. 21. As seen in these configurations, there are two voltage gain extension circuits. First circuit is voltage multiplier cell that includes the secondary winding of the coupled inductor. This seconder winding of the coupled inductor can be connected only in two cascade forms in the boost converter. One of the cascade connection form is to integrate the secondary winding with input section of the boost converter. The other form is series-connection with output section of the boost converter. Second, voltage gain extension cell can represent voltage lift cell or voltage multiplier cells based on Cockcross-Walton, and Dickson voltage multipliers. Likewise, there are two stacked connections of secondary winding of the coupled inductor. So, secondary winding of the coupled inductor is stacked at the input section or output section of the boost converter.

The interleaved classes of these cascade connections can be configured as shown in Fig. 19c and Fig. 19d. The interleaved classes of these stacked connections can be configured as shown in Fig. 20c and Fig. 20d. With these interleaved strucure, input current ripple is reduced and current stress is distributed on each branch of the interleaved converter, power level can be increased due to the shared input power between individual boost converter of the interleaved boost converter. So, they are suitable for high power application. Moreover, few distinguishing solutions are presented in sections below for the performance improvements of these converters. Finally, the general configuration of the integrated boost converter which is another option for the coupled inductor boost converters to reduce input current ripple can be derived as shown in Fig. 21.

General configurations of the sepic converter with coupled inductor are shown in Fig. 22 and Fig. 23. Secondary winding of the coupled inductor can be cascade connected to either input section, middle section, output section or a clamp circuit as shown in Fig. 22a, Fig. 22b, Fig. 22c, and Fig. 22d respectively. The stacked connection forms of secondary winding in the sepic converter with coupled inductor is configured as shown in Fig. 23. So, secondary winding coupled inductor can be stacked at output section or clamp circuit of the converter.

Section 6. 3, as a final section, presents distinct interleaved and inter-coupled inductor converter classes. First, authors in

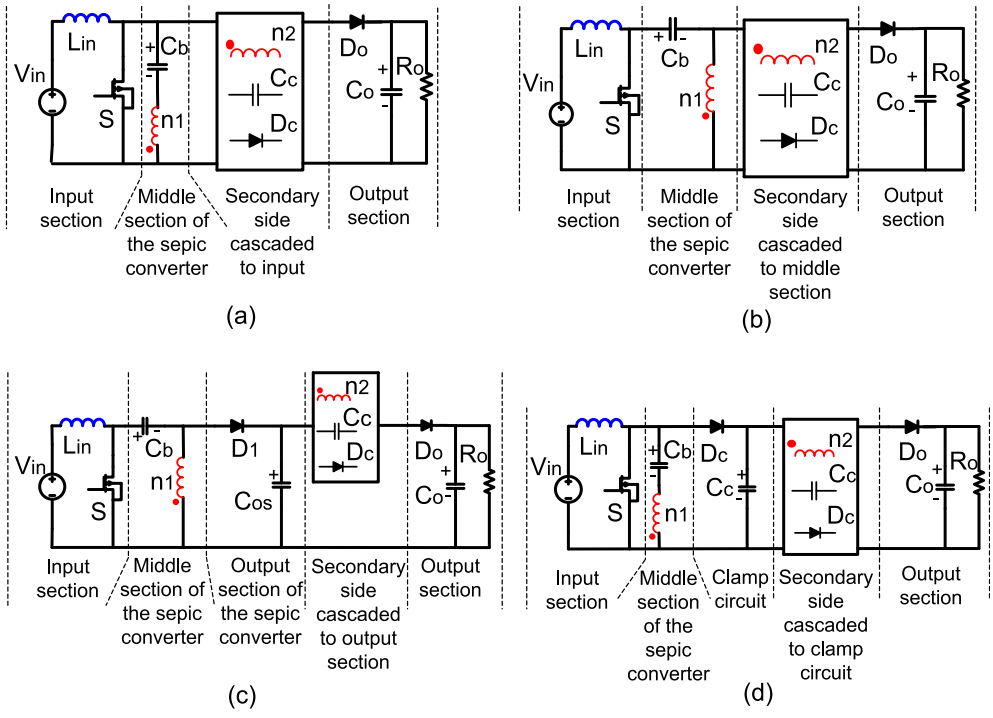

Fig. 22 General configurations of the cascaded coupled inductor sepic. (a) Sepic converter with cascade connected coupled inductor to input section. (b) Sepic converter with cascade connected coupled inductor to middle section. (c) Sepic converter with cascade connected coupled inductorto output section. (d) Sepic converter with cascade connected coupled inductorto clamp circuit.

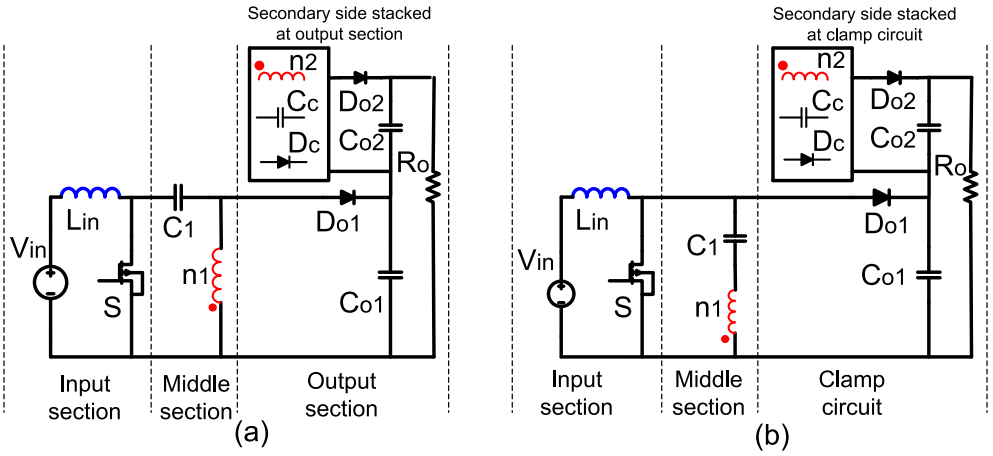

Fig. 23 General configurations of the stacked coupled inductor with sepic converter. (a) Sepic converter with stacked coupled inductor at output section. (b) Sepic converter with stacked coupled inductor at clamp circuit.

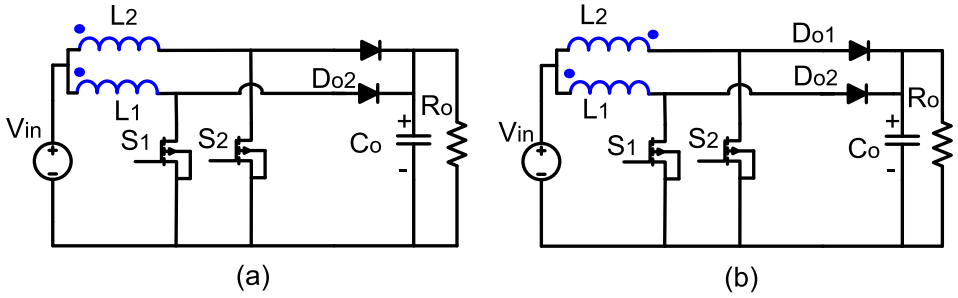

Fig. 24 Interleaved and inter-coupled inductor boost converter (a) direct coupling, (b) inverse coupling.

[48] proposed interleaved structure by integrating inductor modules into magnetic core constitutes of one middle leg without air gap and two morelegs with windings. As compared with the discrete inductor scheme, the flux ripple through the middle leg of the magnetic core and input current ripple are reduced in interleaved structure, thus reduces the size and power losses. Then, researchers in [135] enhanced the structure by introducing an air gap in the middle leg to achieve adjustable coupled inductance. Consequently, various equivalent inductors are obtained in different dynamic operation range of the converter. This leads to manipulate the current ripple in each operation range as well as input current ripple. Based on coupled inductance and duty cycle, a lower input current ripple and a lower inductor current ripple in the converter with inverse coupling inductor (Fig. 24b) is achieved as compared to converter with noncoupling inductor module integrated into one magnetic core [135]. In converter with direct coupling inductor (Fig. 24a), mutual inductor are operated with doubled switching frequency. In order to improve the input current ripple, power density must be increased.

Circuits with low input current ripple components operate with doubled switching frequency are projected with direct coupling and inverse coupling inductor (vide Fig. 24). These converters can be utilized for high power applications, as the two switches divide the input current. This allows the current through the individual interleaved unit to discontinue while input current is in continuous current mode. Therefore, Zero Current Switching (ZCS) can be achieved for switches and reverse-recovery loss of output diodes is eliminated.

6.1. Stacked coupled inductor high step-up converters

These class converters can be categorized into converters with stacked coupled inductor at input/output section and converters with reduced input current ripple. General feature of the most of these converters lies in releasing energy of leakage inductance to output. This can enables to use an active clamp cell comprised of output capacitor of the converter and an auxiliary switch Sa which is replaced with the output diode D_o to realize ZVT for both main switch S and auxiliary switch S_a without using an extra active clamp cell. This active clamp cell makes use of the leakage inductor and clamp capacitor to achieve soft switching condition. The phenomena is observed in a lot of proposed converter in literature since it can be easily applied on coupled inductor boost converters.

6.1.1. Converters with stacked coupled inductor at input/output section

Stacked coupled inductors in input section improve input voltage extension in the converters. Few of these are shown in Fig. 25. By using multi-windings coupled inductor in Fig. 25a–d, voltage stress across the output diode D_o, clamp diode D_{c1} and switch S are reduced while voltage gain of the

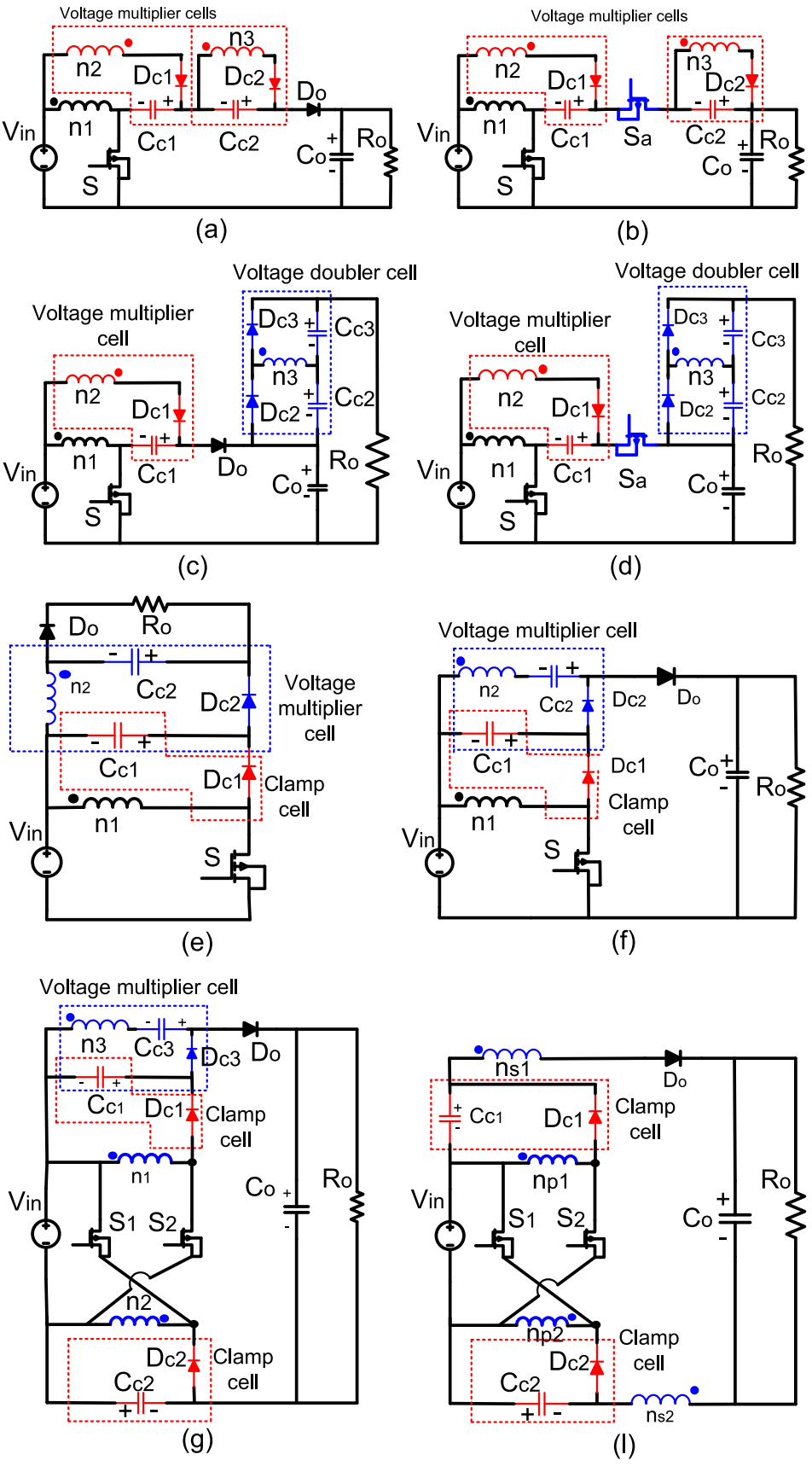

Fig 25 The converters with stacked coupled inductor at input section to improve input voltage extension; (a) converter in [57], (b) converter in [57] with active clamp, (c) converter in [60], (d) converter in [60] with active clamp, (e) converter in [59], (f) converter in [58], (g) converter in [56], (l) converter in [55].

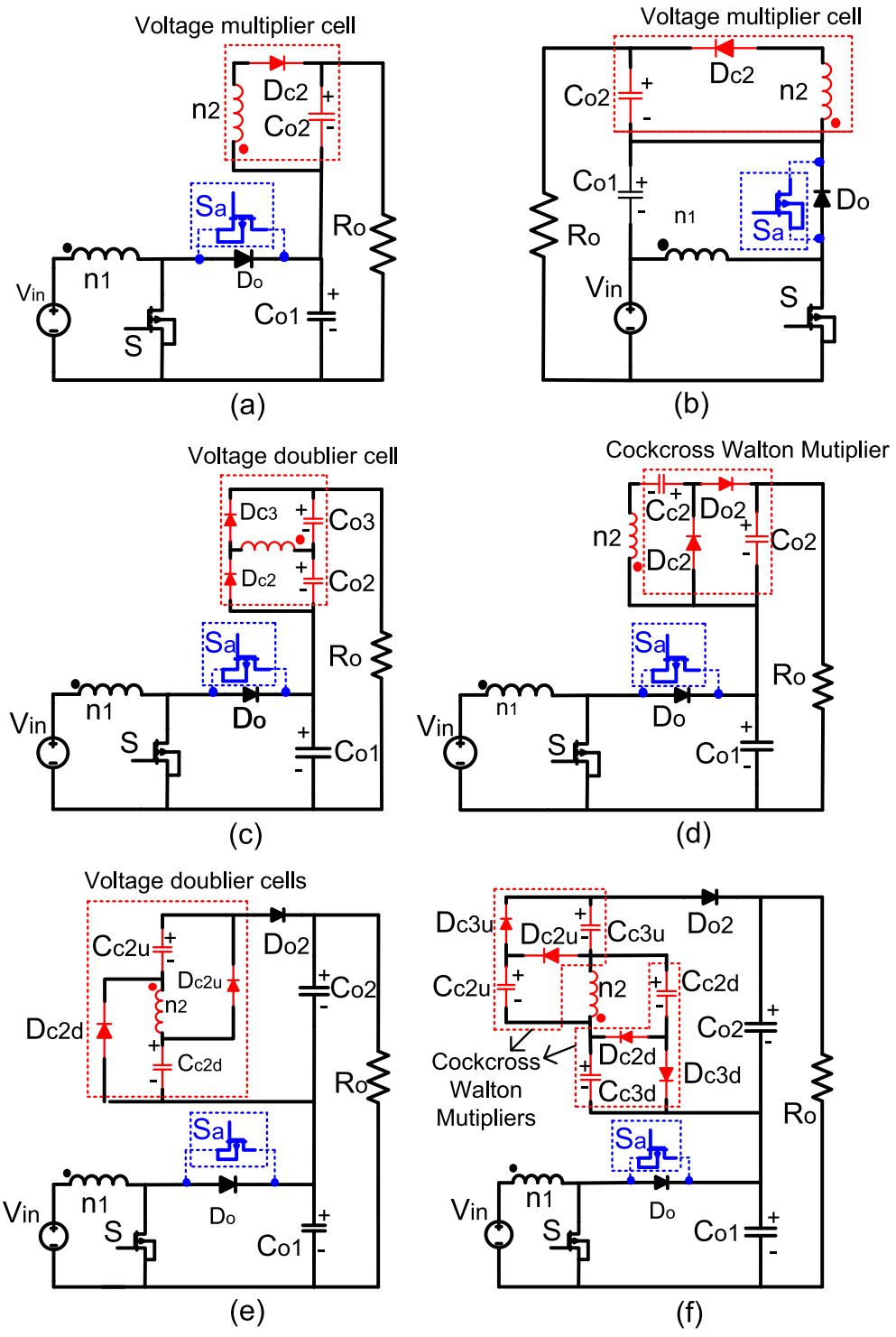

Fig. 26 The stacked coupled inductor boost converters at output section; (a) converter in [62], (b) converter in [61], (c) converter in [63], (d) converter in [65], (e) converter in [67], (f) converter in [68].

converter is extended. However, magnetic core size, cost and leakage inductor are increased. With these topologies in Fig. 25a–d, Leakage energy is directly released to the output of the converter without being hindered by the tertiary winding of the coupled inductor in switch turn-off state. Therefore, reverse current of the output diode Do is recovered due to leakage inductor. In addition to these, voltage spike on all semiconductors of the converters in Fig. 25a–d are suppressed, except for clamp diodes D_{c1} and D_{c2}.

The converter in Fig. 25f can be derived from the converter in Fig. 25e by connecting an output section to clamp capacitor C_{c2} in series. Thus, output capacitor is charged by input voltage V_{in}, secondary windings n_2, and clamp capacitor C_{c2}, resulting in a higher voltage gain. In this converter, clamp

capacitor C_{c1} enables to recovery energy in the leakage inductor, and then, this stored leakage energy in C_{c1} is released to output via capacitor C_{c2}. With this topology, voltage spike across all semiconductors of this converter is reduced. The coupled inductor is operated as forward converter while C_{c2} is charged in switch turn-on. Also, the coupled inductor is operated as flyback converter while its energy is released to output of the converter in switch turn-off. ZCS turn-on and turn-off for power switch is realized by leakage inductors. Input current ripple drawn from source is reduced. Therefore, these features of converter improves system efficiency, utilization of magnetic core and increases power density. By replacing input section of this converter with that in Fig. 18b and using an extra clamp circuit (combining of D_{c2} and C_{c2}) the converter in Fig. 25g is obtained. A typicall example for the use of the active switched coupled inductor network is also given in Fig. 25l. So, the abovementioned features of this network is introduced to these converters. The gain obtained is enhanced for converter in the Fig. 25l by active switched coupled inductor network and a stacked coupled inductor at input section. Clamp circuits recycle the leakage energy, upgrade voltage gain and reduces voltage stress on the output diode. However, output diode D_o has a voltage spike due to leakage inductor in this converter.

Fig. 26 shows the stacked coupled inductor boost converters at output section. For converters in Fig. 26a and Fig. 26b, since primary and secondary side of coupled inductors are employed as boost and flyback converters respectively, voltage gain of converters that equates to sum of these two conventional converters' voltage gain and voltage stress over all the semiconductor devices is lower than output voltage. In such topologies increasing the number of capacitors at output stage in series (shown in Fig. 26b) decreases voltage stress on these capacitor. However, a bigger capacitance value is needed to reduce voltage ripple of output. For the converters in Fig. 26a and Fig. 26b, voltage spike on the diode D_{C2} is high. The voltage spike problem on clamp diodes D_{c1} and D_{c2} is mitigated by voltage doubler circuit used in the converter shown in Fig. 26c, which also increases the voltage gain of the converter and utilization of magnetic core. The voltage gain contributed by Cockcross-Walton voltage multiplier circuit used in Fig. 26d are similar to voltage doubler circuit in Fig. 26c. However, component stresses of this multiplier circuit is different.

The voltage gain is increased and voltage stress on the all semiconductor devices is reduced as two voltage doubler circuits are used, one for upstream circuit consisting of the diode D_{c2u} and capacitor C_{c2u}, and other for downstream circuit consisting of the diodes D_{c2d} and capacitor C_{c2d}. To attain higher voltage gain and lesser voltage stress on the semiconductor devices, voltage multiplier shown in Fig. 26f can be used in converter. For this, Cockcross-Walton multiplier is used as upstream circuit consisting of the diodes D_{c2u}, D_{c3u} and the capacitors C_{c2u}, C_{c3u}while diodes D_{c2d}, D_{c3d} and capacitors C_{c2d}, C_{c3d} are used as downstream circuit. However this increases component count and eventually lowers system's efficiency.

A detailed overview about configurations of these voltage multiplier circuits used for coupled inductors are mentioned in [120]. Lastly, as mentioned above, soft switching performance (ZVT) for main switch S and auxiliary switch S_a in the converters shown in Fig. 26 can be achieved by replacing output diode D_o with auxiliary switch S_a.

6.1.2. Converters with reduced input current ripple

The converters in Fig. 27a, Fig. 27b and Fig. 27e can be derived by two individual units of interleaved converters in Fig. 26c, Fig. 25a and Fig. 26e, respectively. Each unit's coupled inductor windings of interleaved converters are stacked at output of converters, except for converter in Fig. 27b, by sharing voltage multiplier/doubler circuit through winding-cross-coupling. Thus, reducing the number of power devices. Since converters in Fig. 27a, Fig. 27b and Fig. 27e have a symmetrical and modular structure, these can be easily extended to obtain N-phase interleaved converter. The voltage spikes on active switches for converters in Fig. 27 are suppressed due to direct absorption of leakage energy by output capacitors of the converters. By examining the converter shown in Fig. 27e, it concludes that ZVT is realized for all active switches while replacing output diodes with auxiliary switch S_a in the individual interleaved unit of converter. In the converters in Fig. 27c, Fig. 27d and Fig. 27f, output capacitors of the individual boost unit are connected in series at output of the converter. A similiar approach is observed in [146]. This increases the voltage gain, however, duty cycle must be greater than 0.5 and modular structure is impaired in these converters. The voltage spike across the diodes of the voltage multiplier/-doubler circuits of the converters in Fig. 27 cannot be suppressed, except for the converter in Fig. 27c and Fig. 27e.

Fig. 28 shows the integration of the boost converter and stacked coupled inductor boost converter. For continuity of input current, a boost converter can be integrated with converter shown in Fig. 26a to derive the converter (shown in Fig. 28a) to form a reduced input current ripple. A typical example is shown in Fig. 28b. This results in a higher voltage gain with quadratic feature to avoid extreme duty cycle. However, a lower system efficiency is obtained due to increased power process stages and semiconductor devices (D_1, D_2) located in main power branch.

Sepic converter with coupled inductor (vide Fig. 29) is another candidate that implies low input current ripple. Voltage doubler circuits in these converters are stacked at clamp capacitor. Compared with cascade connected converters in Fig. 28, these converters have low voltage gain. However, a built-in transformer in middle section of the sepic converter is always in form of a high-pass and component number in the main power branch is less than that of the cascade connected converters. So, with topology in Fig. 29 system efficiency is increased. As observed, the generalized active circuits can be also applied to sepic converter in Fig. 29a to realize ZVT for both switches S and S_a. The converter in Fig. 29b constitutes a resonant tank that provides a quasi-resonant operation between the two energy storage components by balancing C_r and leakage inductor of the transformer at switch turn-on state. This makes current sinusoidal in primary and secondary side of transformer. Thus alleviating switching losses, conduction losses of the switch and reverse recovery problem of diode of the voltage doubler circuit. However, there are medium level voltage spikes across the switch.

Performance comparison of the converters with stacked coupled inductor chosen from section 6.1 is demonstrated in Table B in appendices.

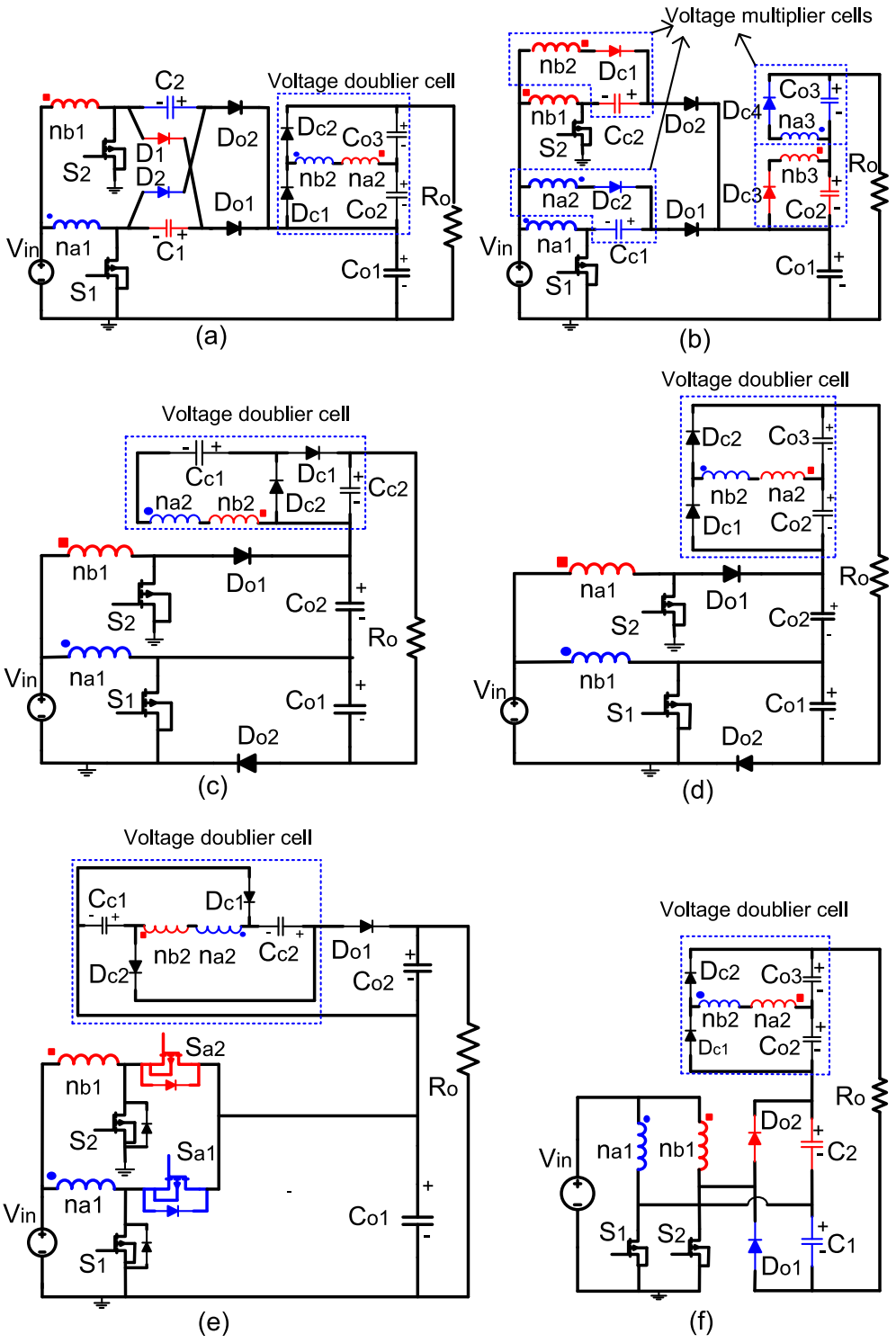

Fig. 27 Interleaved converters with stacked coupled inductor; (a) converter in [71], (b) converter in [72], (c) converter in [73], (d) converter in [75], (e) converter in [74], (f) converter in [76].

6.2. Cascaded coupled inductor high step-up converters

There are two possible cascade-connection types of the coupled inductor for boost converter; connection to input section or connection to output section of the converter. Whereas there are four possible cascade-connection types of the coupled inductor for sepic converter; connection to input section, middle section, output section or clamp circuit of the converter.

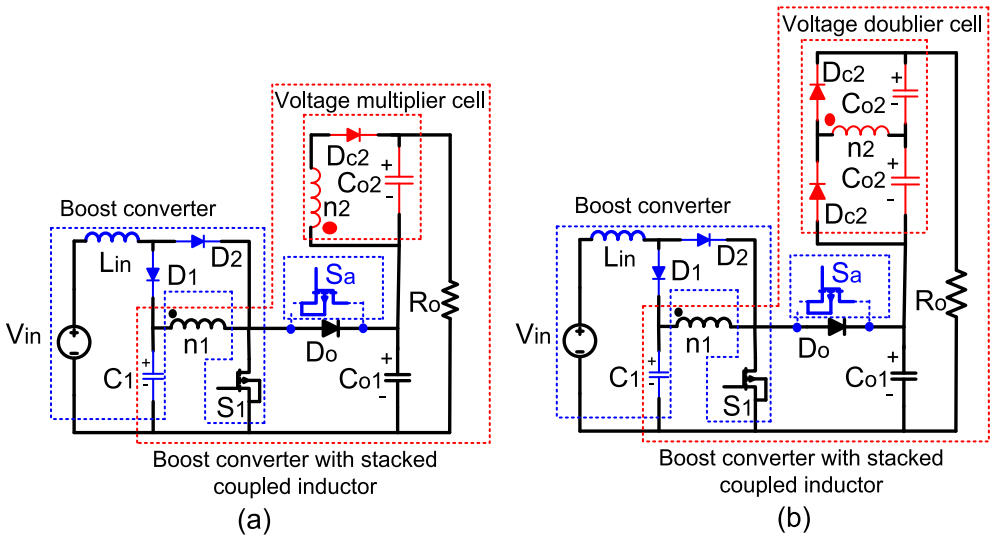

Fig. 28 Stacked coupled inductor boost converters with integrated Boost; (a) converter in [80], (b) converter in [81].

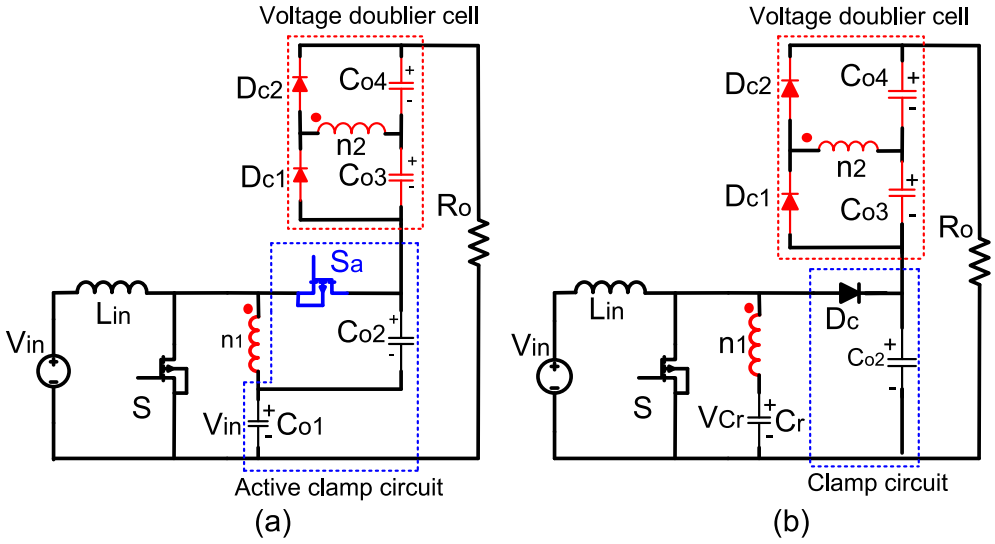

Fig. 29 Sepic converters with stacked coupled inductor; (a) converter in [82], (b) converter in [83].

6.2.1. Boost converters with cascaded coupled inductor to input/output section

Fig. 30 shows the boost converter with cascade-connected coupled inductor to input section. The converter in Fig. 30a like that in [8] has the presented all merits and demerits of the coupled inductor before. These penalties are alleviated by various proposed clamp and voltage multiplier circuits which also results in a higher voltage gain with a reasonable turn ratio. An advantage of these converters in which coupled inductor is cascade-connected to input section is that the clamp capacitor Cc can be associated with voltage multiplier cell including secondary side of the coupled inductor to improve voltage gain.

In Fig. 30b, leakage energy is absorbed by clamp capacitor C_c for recycling this energy by suppressing the voltage spike on switch S. Voltage across this clamp capacitor C_c is contributed to voltage gain of the converter by charge pump consisting of capacitor Cpump and diode Dpump. However, this charge pump produces a current pulse that flowed through switch S and diode Dpump, clamp capacitor C_c and capacitor C_{pump} in series at turn-on state, resulting in high conduction losses. Association of this charged pump cell, clamp cell and secondary side of the coupled inductor as shown in Fig. 30c increases voltage gain of the converter, and suppresses the current pulse due to the leakage inductor. Besides, voltage spike on the output diode D_o is suppressed.

The typical associations of the clamp circuit and voltage multiplier circuit can also be observed in Fig. 30 except Fig. 30(a, g, l) as coupled inductor operates as flyback and forward transformer to transfer the energy. But, similiar energy transfer mechanism is observed in Fig. 30 (g and l). Therefore, magnetic core size the energy stored in the magnetic core is reduced and utilization of magnetic core is increased. In Fig. 30 (g and l), since coupled inductor is cascade-connected to input section of the converter, voltage across switch and secondary windings of coupled inductor together can be

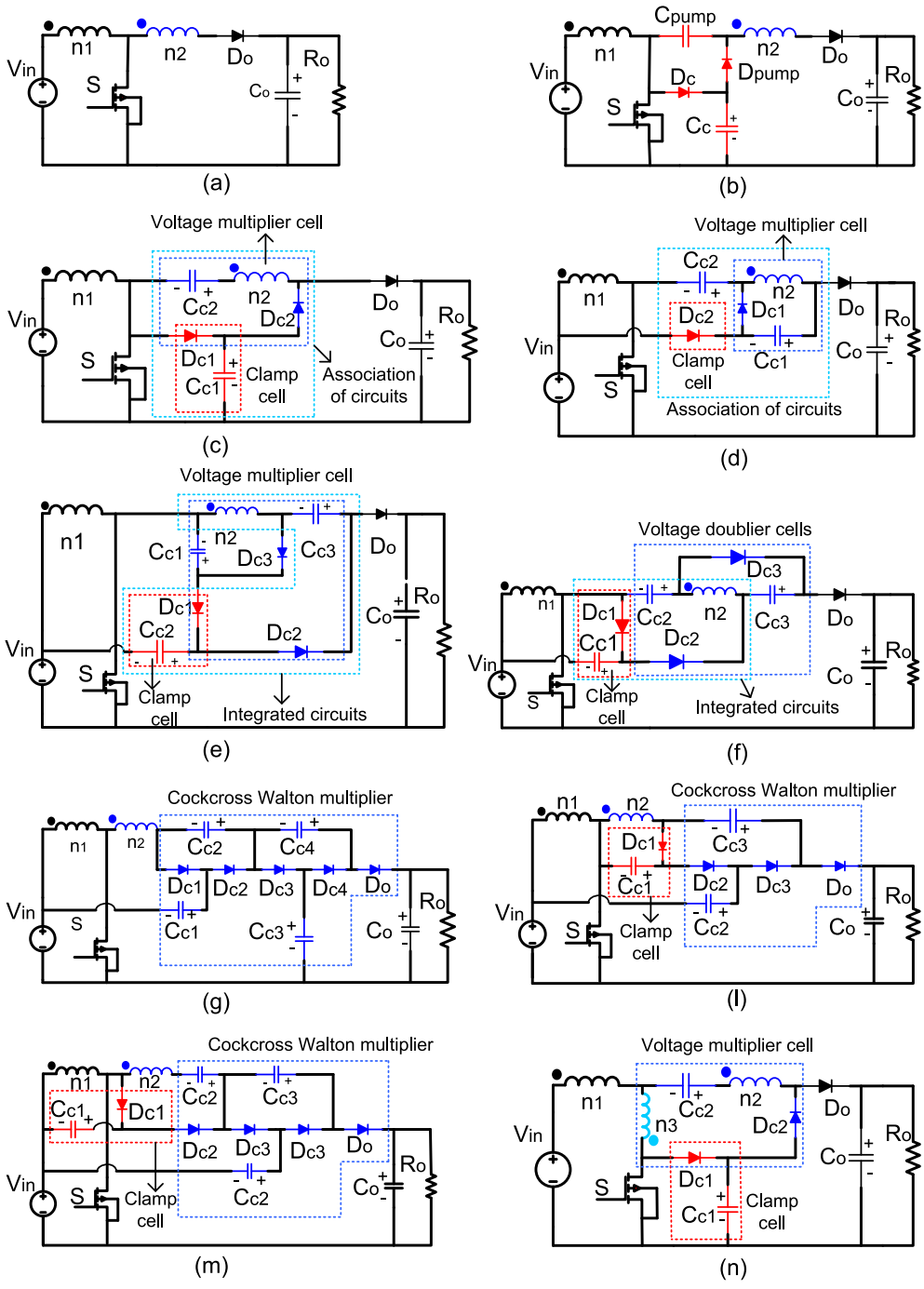

Fig. 30 Cascade-connected coupled inductor boost converters to input section. (a) Converter in [91]. (b) Converter in [92]. (c) Converter in [93]. (d) Converter in [97]. (e) Converter in [99]. (f) Converter in [98]. (g) Converter in [100]. (l) Converter in [101]. (m) Converter in [102]. (n) Converter in [85].

employed as an alternative source of voltage multiplier circuit in order to extend its amplitude. Thus, Cockcross Watson multiplier is applied on output section of the converter to attain a high voltage gain and to decrease voltage stress on the semiconductor devices in Fig. 30(g-m). However, high componunt counts on main power branch reduce the system efficiency. The topological difference between in Fig. 30g an Fig. 30l is that, in Fig. 30l, the clamp circuit is solely used to suppress voltage spikes at medium level on the switch S. By replacing input section of the converter in Fig. 30c with coupled inductor inverse network shown in Fig. 18c, converter in Fig. 30n can be achieved.

In the converters shown in Fig. 30d, Fig. 30e and in [140], secondary windings of the coupled inductor are quantitatively employed more as a flyback converter than forward converter and vice versa is observed in converters of Fig. 30f. This implies that, for instance, comparing the converters in Fig. 30f and Fig. 30e, voltage gain of the converter in

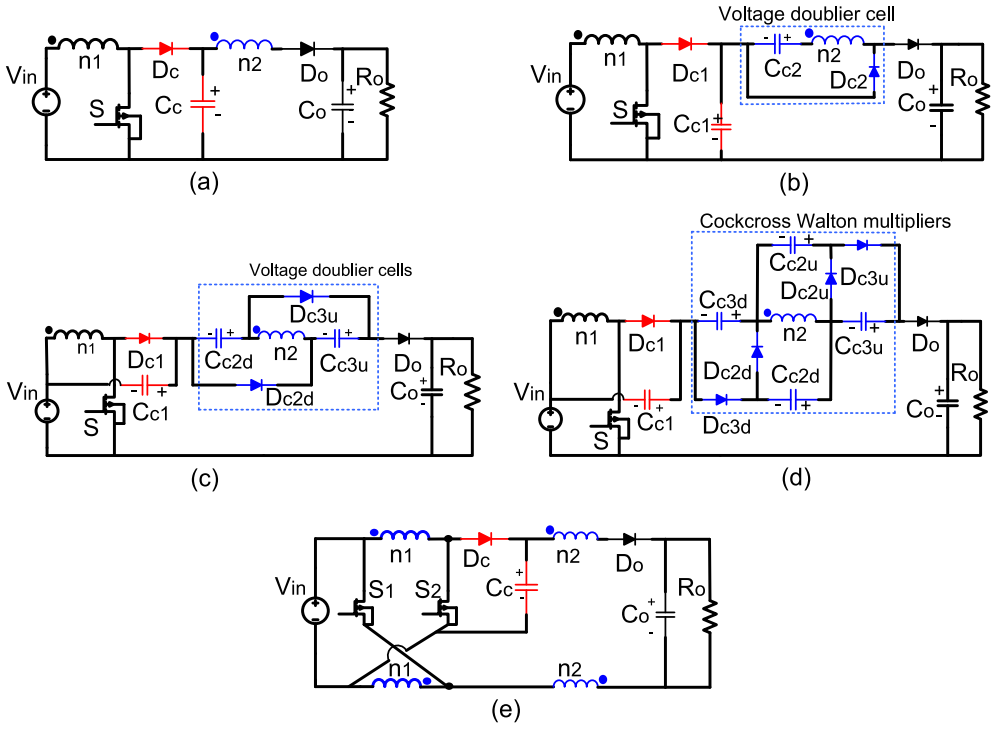

Fig. 31 Cascade-connected coupled inductor boost converters to output section. (a) Converter in [108]. (b) Converter in [109]. (c) Converter in [110]. (d) Converter in [111]. (e) Converter in [87].

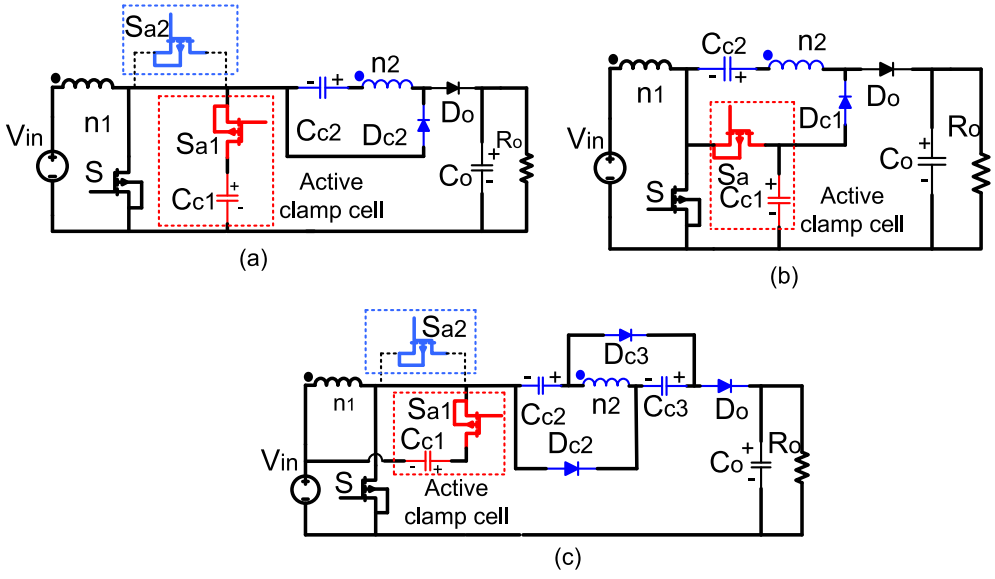

Fig. 32 Cascaded coupled inductor boost converters with active clamp cell. (a) Converter in [94], (b) Converter in [95], (c) Converter in [96].

Fig. 30e is higher than Fig. 30f when duty cycle is larger than 0.5. When, duty cycle is exactly 0.5, the voltage gains of these converters are similar. On the other hand, the voltage gain of the converter in Fig. 30m is higher than the converter in Fig. 30e if duty cycle is less than 0.5. In addition to these, the number of capacitors on main power line in converter (shown in Fig. 30e) is less than the converter in Fig. 30f, whereas the voltage stress across capacitors on main power path of converter in Fig. 30e is higher.

Fig. 31 shows the boost converters with cascade connected coupled inductor to output section. In the converter presented in Fig. 31a, leakage energy is recycled to output of the boost converter same like its stacked counterpart where coupled inductor is cascade-connected to output section of the

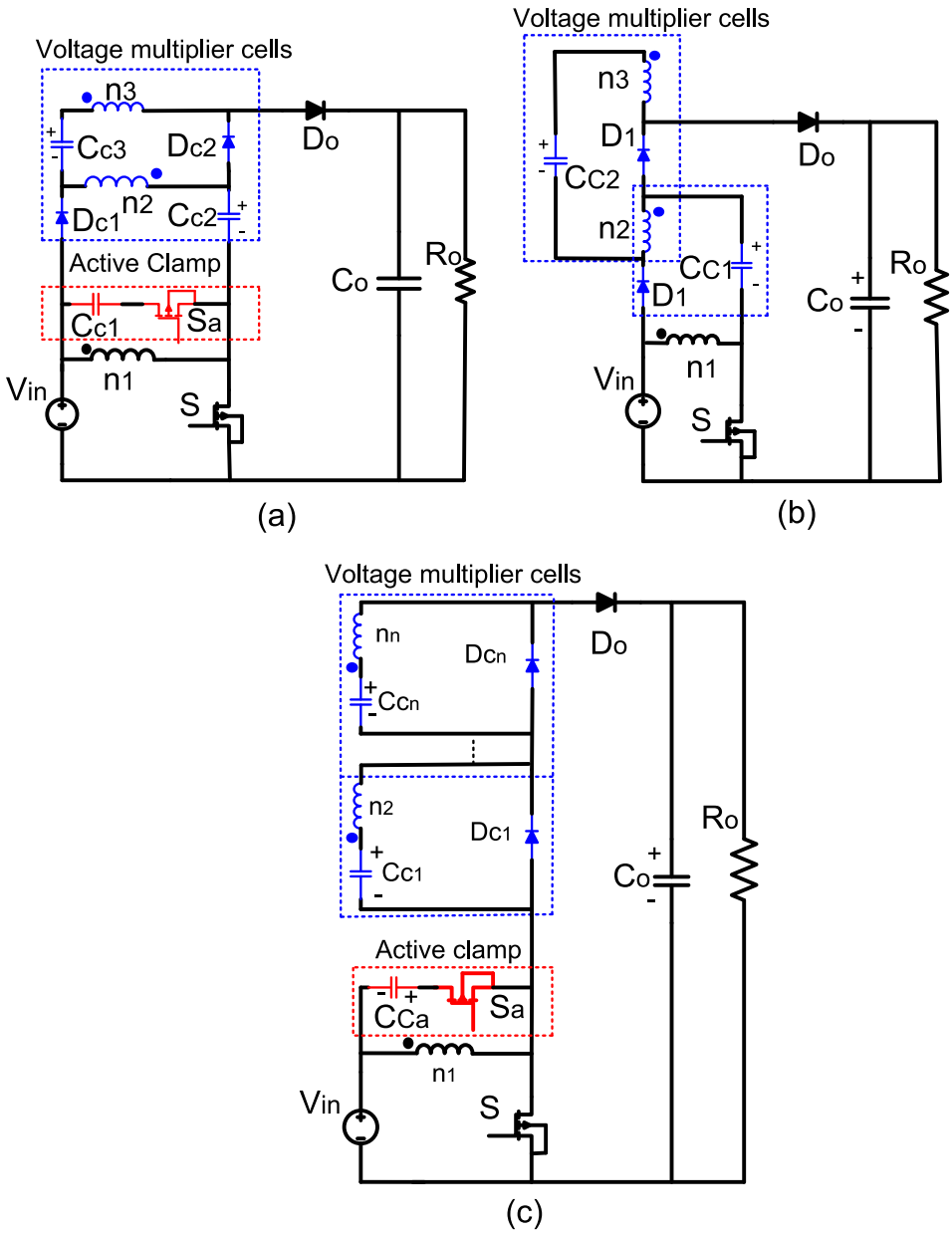

Fig. 33 Cascaded coupled inductor boost converters with multi-winding. (a) Converter in [89]. (b) Converter in [90]. (c) Converter in Fig. 32 with multi-winding.

converter. So, the output capacitor and diode of the boost converter are used as clamp circuit. Stacked counterparts of the converters in Fig. 31a–d are the converters in Fig. 26a and Fig. 26d–f, respectively. When compared with corresponding stacked counterpart, component stresses of the converter such as voltage/current stresses on capacitors exhibit different values. In Fig. 31e, input section of the boost converter is replaced with active switched coupled inductor network and multi-windings of coupled inductor are cascaded to increase the voltage gain. Voltage spikes on power switches S_1 and S_2 can be suppressed due to the leakage energy and recycled by just one clamp circuit. However, output diode has a voltage spike due to the leakage inductor.

Switching losses are the most common problem in above-mentioned converters. So, a Soft switching method used widely in converters with coupled inductor is illustrated in Fig. 32. With this soft switching performance, ZVT can be realized for main switch S and auxiliary switch S_a. The auxiliary switch S_a can be located in two different path, either at location of switch S_{a1} or S_{a2} as shown in converters in Fig. 32a and Fig. 32c. If auxiliary switch S_a is located at switch S_{a2} for active clamp cell, less voltage stress on output diode D_o and minimal RMS current flowed through active switch S_a are obtained as advantages [112]. If auxiliary switch S_a is placed at switch S_{a1} for active clamp cell, clamp capacitor C_{c1} can be associated with the voltage multiplier cell to extend voltage gain of the converter as shown in Fig. 32b.

Multi-winding coupled inductor is a flexible and compact structure as shown in Fig. 33 is used to extend voltage conversion ratio of the converter. Use of multi-winding coupled

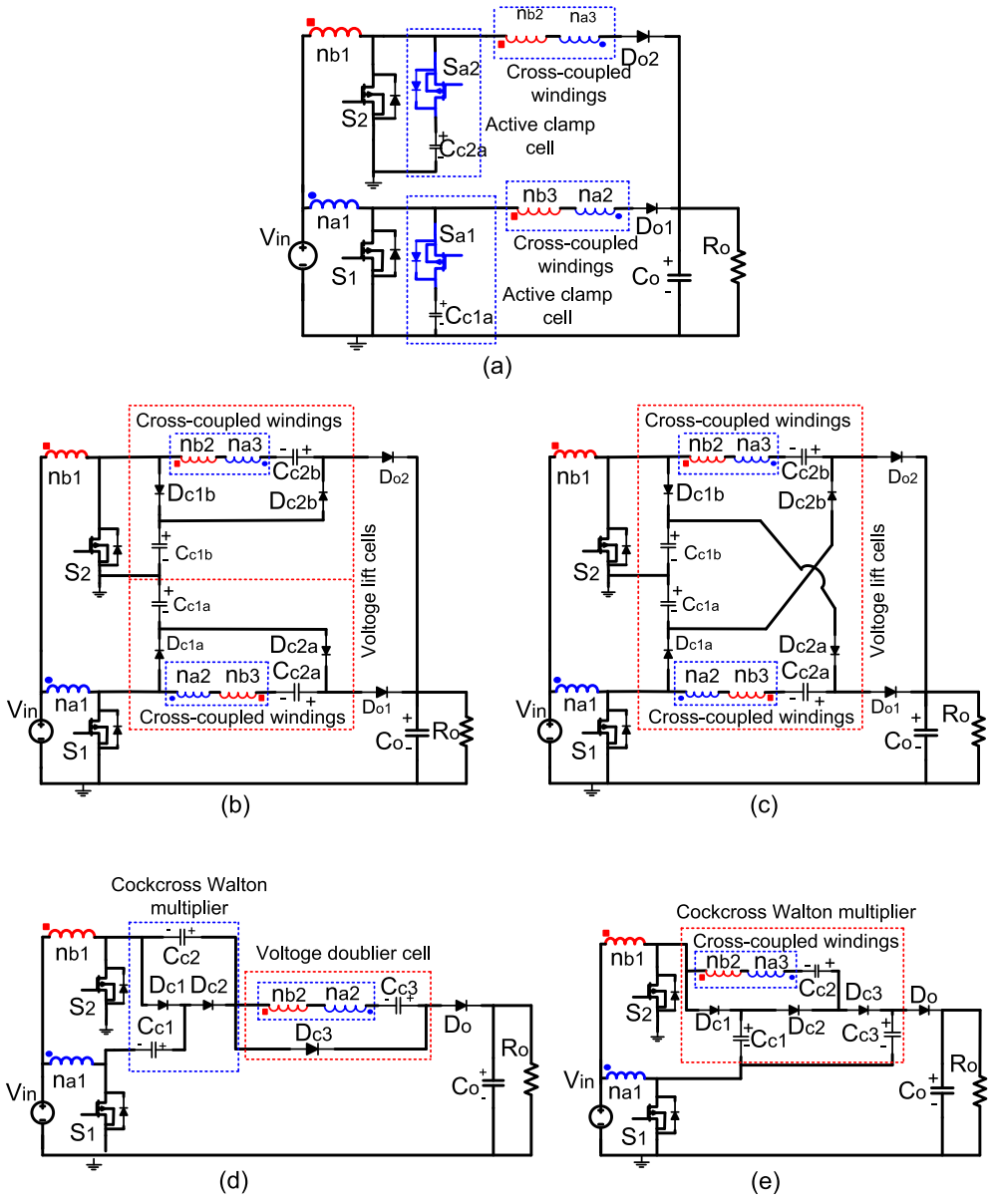

Fig. 34 Interleaved boost converters with cascaded coupled inductor to input section. (a) Converter in [114]. (b) Converter in [115]. (c) Converter in [118]. (d) Converter in [120]. (e) Converter in [119].

inductors is more reasonable than a coupled inductor with high turn ratio since it allows distributed voltage stress of the rectifier diodes and decreases the leakage inductance. The converters presented in Fig. 33a and Fig. 33b are proposed as different topologies, however, the only difference between them is the use of active clamp cell in Fig. 33a. While in Fig. 33b, voltage spike on all semiconductor devices cannot be suppressed fully, but stays at medium level. By using this active clamp cell in converter in Fig. 33a, not only ZVT is realized for both power switches S and S_a, but also voltage spike on all semiconductor devices are suppressed except for diode D_{c1}. For topology in Fig. 33c, voltage gain of the converter is lower than the others. However, with using active clamp cell, voltage spike on all semiconductor devices can be suppressed.

6.2.2. Converters with reduced input current ripple

In interleaved converters in Fig. 34 and Fig. 35, cross-coupling windings not only enhance the voltage gain of the converter but also the voltage spike and voltage stress on the output diode D_o. Duty cycles of these converters are limited to be higher than 0.5.

In the interleaved converters displayed in Fig. 34, secondary windings of coupled inductors are cascade-connected to input section of the interleaved boost converter through the cross-coupling. This allows the integration of voltage multiplier cell to cross-coupling windings of the coupled inductor and clamp cell. In other words, this grants the voltage amplitude extension of voltage multiplier cell by adding voltage across the power switches. By using active clamp cell in

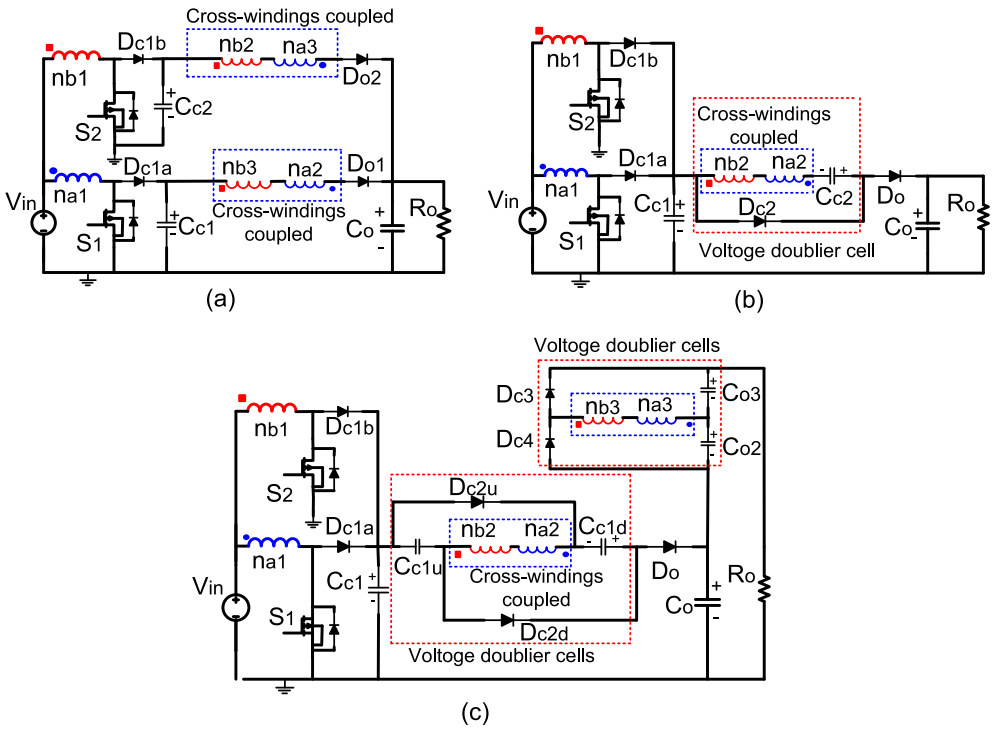

Fig. 35 Interleaved coupled inductor boost converters with cascaded to output section. (a) Converter in [116]. (b) Converter in [113]. (c) Converter in [79].

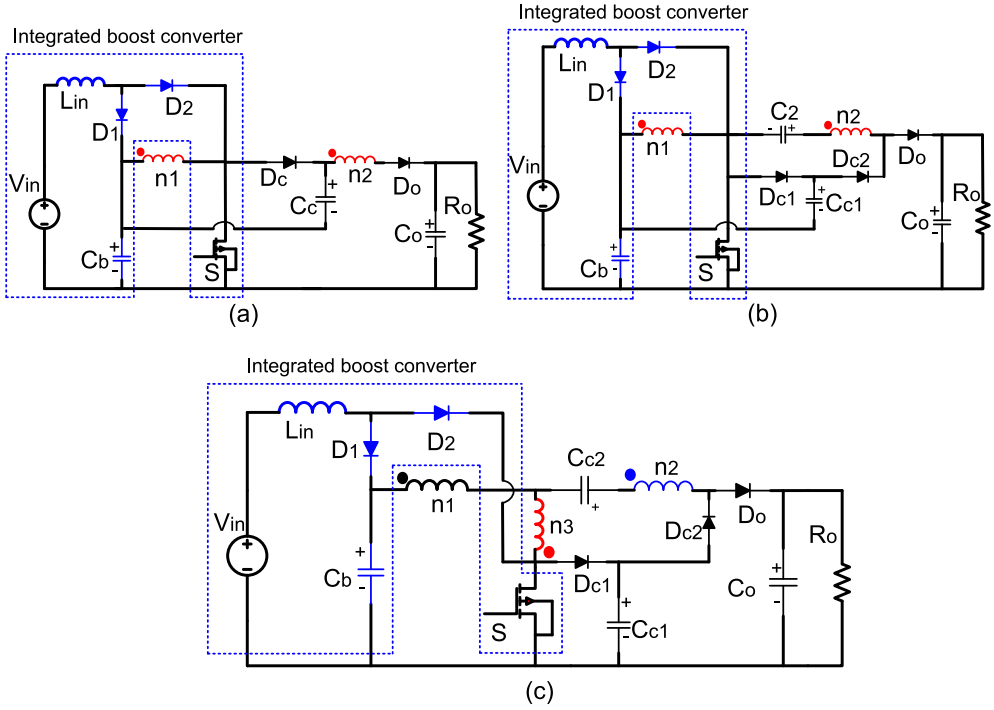

Fig. 36 Cascaded coupled inductor boost converters with integrated Boost. (a) Converter in [122]. (b) Converter in [125]. (c) Converter in [86].

converter of Fig. 34a, switching losses can be eliminated. However, in this converter, voltage stress and voltage spike on the output diode is high. With voltage lift cells consisting of association of voltage doubler circuit and clamp capacitor in the individual boost cells of the interleaved converter in Fig. 34b, voltage gain of both converters is increased and voltage stress on output diodes D_{o1} and D_{o2} is reduced. As it can be seen in Fig. 34b and Fig. 34c the variation in converters is

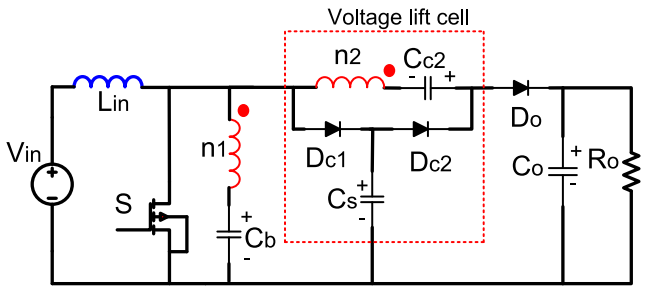

Fig. 37 Sepic converterwith coupled inductor cascade-connected to input section [126].

obtained by replacing the clamp capacitors in the voltage lift cells with each other, voltage gain in each branch of the interleaved converter in Fig. 34c remains same, even though the switches of the interleaved converter have a different duty cycle range. So, a circulation current can be suppressed and the branch current auto balance is obtained. In converter in Fig. 34d, in addition to voltage doubler cell with cross-coupled windings, Cockcross Walton multiplier is also employed to increase voltage gain of the converter. In the converter designed in Fig. 34e, by contributing the cross-coupled windings in the Cockcross Walton multiplier to extend voltage amplitude of alternative source of voltage multiplier cell, voltage gain of the converter is increased. However, in the converters of Fig. 34d and e, there is no current balance between the branches of the interleaved converter. Except for the converter in Fig. 34a, voltage spikes on output diodes as well as on all diodes of the all voltage doubler cells of converters in Fig. 34 are at the medium level.

Fig. 35 shows the interleaved boost converters with cascaded coupled inductor to output section. So, Leakage energy is inherently absorbed by capacitor at the output of the interleaved converter. Cross windings coupled inductor is added to output section of the individual boost cells of the interleaved boost converter in Fig. 35a. So, leakage energy is absorbed by both capacitors, C_{c1} and C_{c2} and voltage stress on the output diode is reduced. However, voltage spike on the output diode is high. With topology in Fig. 35b, a common cross-coupled windings is added to output section of the interleaved boost converter without using the multiwindings coupled inductor as in the converters of Fig. 35a, which resulted in a lower magnetic component size, diode and capacitor count. Its typical examples can be found in Fig. 34d and Fig. 34e. However, it leads to an increased output voltage ripple compared with the converter in Fig. 35a. In the converter in Fig. 35c, by using voltage doubler cells, obtained voltage gain is increased. Except for the converter in Fig. 35a, voltage spikes on output diodes along with all diodes of the all voltage doubler cells of converters in Fig. are at the medium level.

Fig. 36 shows the cascaded coupled inductor boost converter with integrated boost converter. The converters in Fig. 36a, Fig. 36b, and Fig. 36c can be derived from converter in Fig. 31a, Fig. 30, and Fig. 30n. by integrated boost converter, respectively, resulting in high voltage gain and a low input current ripple.

Figs. 37-39 reveals that the coupled inductor sepic converter is inherently provided with a low current ripple only by changing the inductor in the middle section of sepic converter with a coupled one. With topology in Fig. 37, storage capacitor Cs absorbs leakage energy and realizes ZVS turn-off for switch S. Coupled inductor is cascaded to the input section of sepic converter. So, voltage gain is increased by voltage lift cell. Voltage stress on the all semiconductor devices are less than the output voltage and voltage spike on the all semiconductor devices is suppressed.

In the converters appeared in Fig. 38 coupled inductor is cascade-connected to clamp circuit. In the modified sepic converter in Fig. 39a, positive alternanace of capacitor C_1 is changed by connection form of the clamp circuit. In this converter, the secondary side of the coupled inductor is cascade-connected to middle section of the sepic converter. So, this positive alternanace of capacitor C_1 changed by connection-form of the clamp circuit contributes to voltage gain of this converter. A similiar modified sepic converters have been proposed in [141] and [143]. The topology of the cascade-connection to middle section allows itself to be used by voltage lift cell to upgrade the voltage gain as shown in Fig. 39b. In converters in Fig. 38 and Fig. 39, voltage stress on all semiconductor devices is less than the output voltage while voltage spikes are suppressed except for the output diode Do of the converter in Fig. 39a.

Performance comparison of the converters with cascaded coupled inductor chosen from section 6.2 is demonstrated in Table C in appendices.

6.3. Interleaved and inter-coupled boost converters

There are two coupling methods for these class converters; direct coupling and inverse coupling (vide Fig. 24). Improved voltage gain of the converter with direct coupled inductor in Fig. 40a and [148] lies in increasing effective duty cycle which is summation of duty cycle values of the switches in switching period. Due to the leakage inductor of the coupled inductor, switches realize ZCS turn-on and output diodes realize ZCS turn-off in this converter. In the converter in Fig. 40d, since

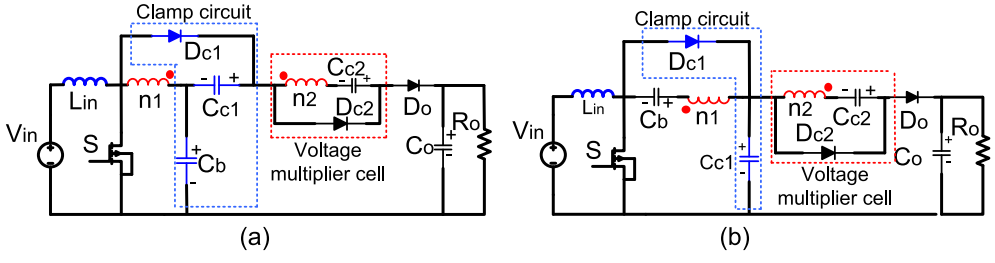

Fig. 38 Sepic converters with coupled inductor cascade-connected to clamp circuit. (a) converter in [124].(b) Converter in [125].

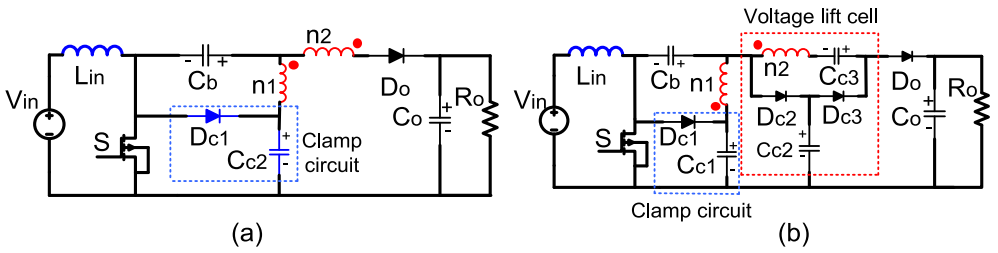

Fig. 39 Sepic converters with coupled inductor cascade-connected to middle section. (a) converter in [128]. (b) Converter in [127].

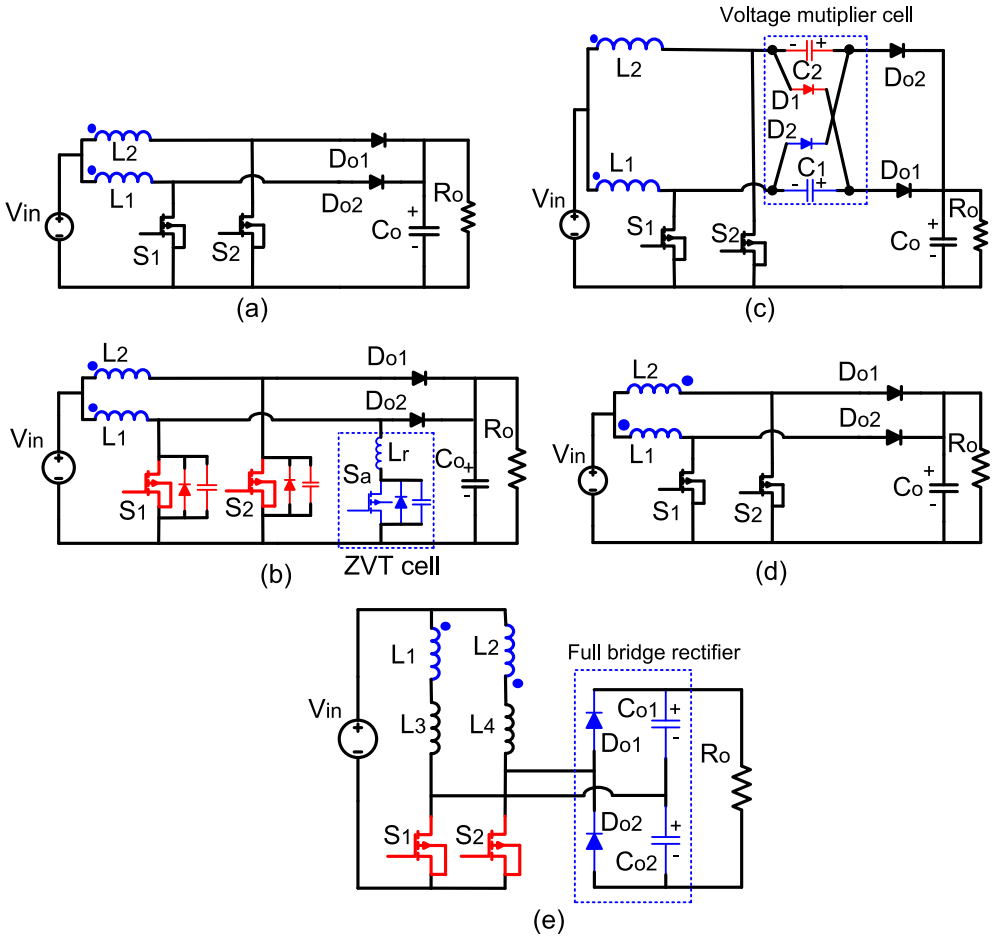

Fig. 40 Interleaved and inter-coupled boost converters. (a) Converter in [129]. (b) Converter in [130]. (c) Converter in [131]. (d) Converter in [132]. (e) Converter in [133].

individual boost converter circuits operate in DCM, switches realize ZCS turn-on and output diodes realize ZCS turn-off. In converters shown in Fig. 40a and Fig. 40d, individual boost converter cells are actually operated in DCM. As far as input currents of these converter are concerned, these appear to operate in CCM. In [130], utilizing of the characteristic of the converter in [129], Zero voltage transition (ZVT) can be achieved by just a single auxiliary resonant module for the switches S_1 and S_2 under the condition in which duty cycle is set to be less than 0.5. However, the energies of parasitic capacitors of switches cannot be recycle. These energies are lost by expending on parasitic resistance of the switches through the auxiliary inductor of soft switching module.

Voltage stresses on switching devices in abovementioned converters are equal to output voltage. In [131], the converter's voltage gain is improved without effecting the modular structure of interleaved coupled inductor boost converter and voltage stress on the switches and output diodes are decreased with the use of voltage multiple circuit (see Fig. 15d). In this converter, switches S_1 and S_2 are complementary to each other and activated in a way ensuring ease of converter control, whereas, the current autobalance between the branches of the interleaved boost converter is ensured by means of the switching capacitor even in the different duty cycles of the switches. In [133], full bridge rectifier is put to use to increase voltage gain and decrease voltage stress on the switch devices.

With this topology, when there is merely an overlapping between the conduction times of switches, the energy is stored in the inductors L_3 and L_4. When one of the switches is turned off, the energy stored simultaneously in this inductor is also discharged simultaneously due to the current mirror effect of the coupled inductor named as auxiliary transformer. Therefore, the regulation of output voltage can be achieved at a wide load range. Moreover, full bridge rectifier served to increase voltage gain. However, a hard switching problem exists in the converter and input current ripple is higher than the inductor currents ripples.

Performance comparison of the converters with interleaved and inter-coupled coupled inductor chosen from section 6.3 is demonstrated in Table D in appendices.

7. Performance evaluation of high step-up converters

For performance comparison of the overviewed topologies, detailed performance parameters in terms of component number, voltage conversion ratio, switch and diode voltage stress, soft-switching performance, and peak efficiency are quantitively reported in Tables A–D. Furthermore, non-isolated high step-up converters are compared by designed and simulated topologies under the same benchmark and specifications. Selected topologies from the abovementioned categories shown in Fig. 1 are that in Fig. 8(c) [23], Fig. 11(b) [40], Fig. 16(e) [52], Fig. 25 (f) [58], Fig. 26 (d) [65], Fig. 30 (f) [98], Fig. 31 (c) [110], Fig. 34 (c) [118], Fig. 36 (b) [125], Fig. 39 (b) [127]. Design specifications by taking care an application instance of PV system in [111] are set as below.

1. 25 V input voltage, 400 V output voltage, 50 kHz switching frequency, 200 W power rating are set. Taking into account of the 200 W power rating for individual boost converter of interleaved boost converters, these converters are set 400 W power rating.
2. Maximum duty cycle is set to be 0.75.
3. Voltage ripple of the capacitor is neglected due to the capasitances of them are large enough. Magnetising inductance of coupled inductor and input inductor are designed to guarantee Continuous Conduction Mode (CCM) operation at 40% of power rating (200 W).

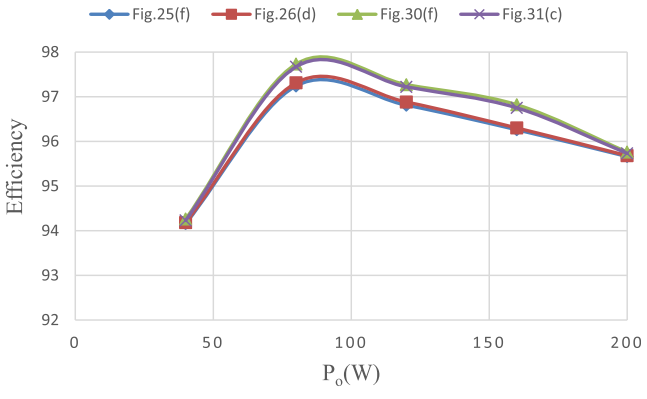

Fig. 41 Efficiency of converters with coupled inductor.

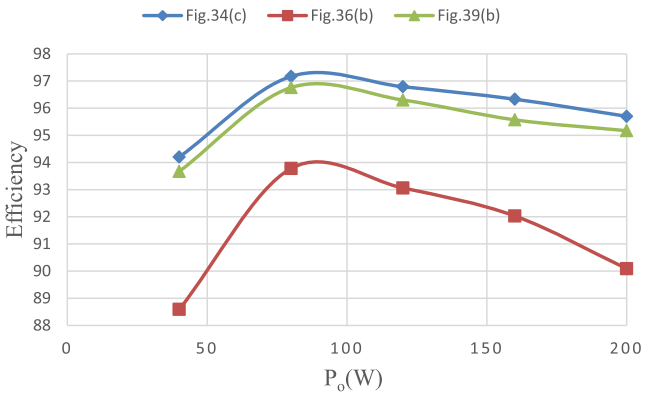

Fig. 42 Efficiency of the coupled inductor converters with low input current ripple.

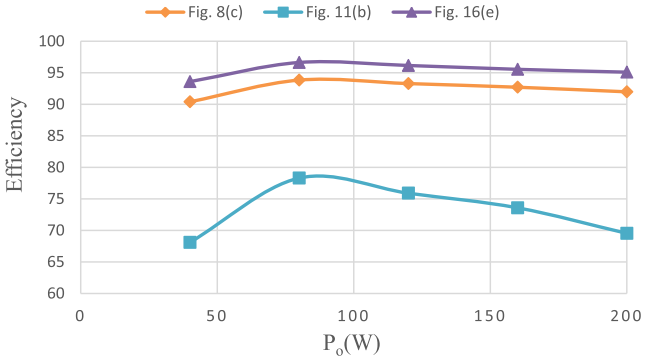

Fig. 43 Efficiency of converters with non-coupled inductor.

Based on the above specifications, the designed converter topologies representing the above mentioned categories is simulated and results are tabulated to compare as shown in Tables E and F in appendices. To ensure relatively an acceptable comparison result for the converter efficiency, power loss is calculated by using simulation data. Similarly, components are selected based on the design and simulation data. These components are listed in appendices. Therefore, power loss of the switches, diodes, coupled inductor and input inductor can be achieved.

Switch loss can be obtained as;

$$P_{S,loss} = I_{RMS}^2 R_{DS,on} + P_{SW} \quad (1)$$

$$P_{SW} = P_{SW,on} + P_{SW,off} + P_C \quad (2)$$

where $R_{DS,on}$ and I_{RMS} are conduction resistance and RMS current of the switch, respectively, P_{SW} is swithcing loss, $P_{SW,on}$, $P_{SW,off}$ and P_C are turn on and turn off loss of the switch, and junction capacitance loss, respectively [137,153].

Diode loss can be calculated as;

$$P_{D,loss} = V_F \cdot I_{F(AV)} + I_{F(RMS)} \cdot r_d \quad (3)$$

where V_F and r_d are forward voltage drop and equvailent resistance of switch, respectively, $I_{F(AV)}$ and $I_{F(RMS)}$ are avarage forward current and forward RMS current of the diode, respectively [153].

Coupled inductor loss can be calculated as;

$$P_{L,loss} = \left(R_{dcp} + R_{acp}\right) \cdot I^2_{p(RMS)} + \left(R_{dcs} + R_{acs}\right) \cdot I^2_{s(RMS)} + P_{fe} \quad (4)$$

$$P_{fe} = V_C K_C f^{\alpha} B^{\beta}_{\max} \quad (5)$$

where R_{dcp}, R_{acp}, R_{dcs}, and R_{acs} represent dc anda ac winding resistance. $I_{p(RMS)}$ and $I_{s(RMS)}$ are RMS current of pimary and secondary winding, respectively. P_{fe} is core loss. V_C is thee core volume. K_c, α and β are presented by the manufacturers [104,137]. Similarly, input inductor loss can be calculated.

Therefore, by using abovementioned equations, simulation data and component data values provided by manufacturers, the efficiency of the selected converters can be estimated as shown in Figs. 41–43.The stacked at input section topology in Fig. 25(f) and stacked at output section topology in Fig. 26(d) has a same voltage convertion ratio, component count, and nearly similiar converter efficiency and component stress. The cascaded to input section topology in Fig. 30(f) and cascaded to output section topology in Fig. 31(c) has similiar converter efficiency and component count. Compared semiconductor rating (ScR) in these converters, topology in Fig. 30(f) has a lower ScR for switch while topology in Fig. 31(c) has a lower ScR for diodes. This is becouse of voltage lift cell used in converter in Fig. 30(f) and this cell contributes to converter a higher voltage gain at the same duty cycle. The low voltage stress on the semiconductor devices is obtained by using voltage multiplier cell in converters in Fig. 30(f) and Fig. 31(c).

Use of the voltage multiplier cells in the converters can reduce turns ratio of the coupled inductor, increase the voltage gain, voltage stress on semiconductor devices and so on. High turns ratio increases the volume and the cost. However, in the converter with low component count in Fig. 30(c), coupled inductor with high turns ratio is in use of the voltage gain and the converter efficiency is still excellent. As a design example in use of coupled inductor, coupled-inductor-inverse-network in converter in Fig. 30(n) increases voltage gain and utilization of the magnetic core and make the system efficiency more perfect.

Fig. 42 shows the effciency of the coupled inductor converters with low input current ripple. A low system efficiency is appeared in coupled inductor converter with integrated boost in Fig. 36(b) due to the high voltage stress on switch and high current stress through including diodes (D_1 and D_2) to input section of the converter. Due to the sepic converter with coupled inductor in Fig. 39(b) has the lowest ScR but two magnetic component, it's efficiency is higher than coupled inductor with integrated boost converter but lower than that in the individual boost of the interleavead coupled inductor boost converter in Fig. 34(c). The topology in Fig. 34(c) has a current auto-balance control, however limitation of the duty cycle is required to be high in this converter. This results in an affecting system efficiency. The interleaved converter with low component count in Fig. 27(d) in the stacked coupled inductor category is a competitive candidate for a high voltage gain and efficiency. Typical examples of this topology are shown in Fig. 27(c) and Fig. 27(f).

Fig. 43 shows the efficiency of converters with non-coupled inductor. the cascaded topology with high voltage gain in Fig. 11(b) has inherently a high ScR. So, the system effciency is quite low. The active switched inductor cell in converter in Fig. 8(c) allows to distrubute the voltage and current stress on the switches. Use of the common voltage multiplier in the interleaved converter in Fig. 16(e) reduces voltage stress on the switch and diode, component count, and ScR. However, limitation of duty cycle of this converter affect the convertion effciency.

8. Summary

The selected solutions for high step-up application depends on the some design constraints to achieve the most reliable, robust and the best performance topology. The voltage gain of the high step-up converters for the renewable energy system is desired to be more than 10. Table-A shows the performance parameter of the converter with transformer-less. In these converters, there is no a need of particular design constraints for the parasitic inductance and input current ripple has emerged by a transformer/coupling inductor. So, converters with current source can be employed with reliability to the renewable energy systems by avoiding the use of big electrolytic capacitors. To achieve high efficiency and performance of the converter, a low voltage stress on the switches, a low duty cycle range and a soft switching cell are needed. Moreover, the increased component count in the main power branch for enhancing the voltage gain decreases the efficiency and in turn increases the cost and bulkiness of the converter.

The use of coupled inductor significantly decrease the component count used in transformer-less converters to have a high voltage gain. In addition to improvements needed for the efficiency and performance in the transformer-less converters, coupled inductor high step up converters also need particular design constraints and improvements about the parasitic inductance, turn ratio of the coupled inductor, input current ripple and much more. Common advantages of these converters are; big voltage gain, a low voltage stress on the switch, alleviation of the reverse recovery problem of the output diode and to achieve the ZVT soft switching performance by applying the active clamp cell. In the majority of the improved converters, leakage energy is recycled and voltage spike on the semiconductor devices is suppressed. In addition to these features, few distinguishing solutions are presented above for; the improvements in performance and the key features. Performance comparison of the topological variations of the coupled inductor high step-up converters in Table-B-C-D are depicted.

9. Conclusion

In the energy conversion systems like renewable energy systems with fuel cell or PV panel, non-isolated high step-up converter is widely employed to reduce cost and to upgrade efficiency of the system. To achieve a high voltage gain and efficiency but with a low cost, the non-isolated high step-up converters are improved by various topologies. With the topologies of switching inductor/capacitor cells, cascaded/stacked and interleaved converters, the voltage gain of the transformer-less converters is extended. General improvements adopted for the efficiency and performance of these converters are: to decrease duty cycle; to reduce the voltage stress on the

switches; to alleviate switching losses and reverse recovery problem by applying the soft switching techniques. The use of a large number of the components in this converter to improve voltage gain is a problem. The voltage gain is improved by utilizing turns ratio of the coupled inductor without using a large number of the component as in transformerless converter.

By applying coupled inductor on step-up DC/DC converters; utilization of magnetic core are improved; voltage stress on the power switch is reduced, and reverse current of output diode can be recovered by leakage inductor. Among the high step-up converter with coupled inductor, boost and sepic converters with coupled inductor are promising candidates. Boost converter with coupled inductor has a high convention ratio, simple structure, low component count and so on. Sepic converter with coupled inductor has a low input current ripple, a transformer inductor in form of high-pass filter.

General improvements for high step-up boost and sepic converter with coupled inductor are: to increase the voltage gain without extreme duty cycle by adjusting the turns ratio of the coupled inductor; to recycle the leakage energy; to suppress the voltage spike; to reduce the voltage stress on power switch and diodes; to improve the utilization of magnetic core. For particularly boost converter with coupled inductor, extra improvement processes are: to reduce input current ripple by integrated boost converter or a interleaved structure; by using the active switched coupled inductor network and coupled-inductor-inverse-network to increase the voltage conversion ratio resulting in the low duty cycle and voltage stress on the switch. So, these converters trend to topologies with switched coupled-inductor-networks/capacitor cell.

Performance comparison of the overviewed topologies are tabulated in Tables A–D in terms of the component number, voltage conversion ratio, switch and maximum diode voltage stress, soft-switching performance, and peak efficiency. The highlights of the reviewed topologies and the prominent topologies are introduced. In addition, Selected non-isolated high step-up converter topologies from abovementioned categories are designed and simulated to compare under the similiar specifications and benchmark. Component count and component stress of these converters are reported in Tables E and F. Power loss of the converters is analized and efficiency of them is graphically presented.

In this paper, a significant majority of the non-isolated high step-up topologies are comprehensively generalized, comparatively evaluated and systematically categorized based on the circuit structure. A well-detailed picture on treatments and general framework for non-isolated high step-up DC/DC converters is provided in this paper.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Appendix. *Performance comparison of the non-issolated high step-up DC/DC converters*

Tables A–D show the performance parameters of the converters chosen from section 1–5, section 6.1, section 6.2 and section 6.3, respectively. It must be noted that the switch voltage stress, the maximum diode voltage stress and some of the peak efficiency values of the converters in this table are taken from figures of the experimental results of the converters as an approximate value for researchers' convenience.

See Table A, B, C, D, E, F.

The follow appendix demonstrates the component lists used in representative converter topologies compared in section 7.

For Fig. 8(c) [23] topology, components are IRFB4127 (MOSFET, for S_1 and S_2), STPS3H100 (diode, for D_1, D_2, and D_3), STTH3R04 (diode, for D_{c1}, D_{c2}, and D_{c3}), and EE34/14/13 (core, for L_1, L_2, L_3, and L_4). For Fig. 11(b) [40] topology, components are IRFP460 (MOSFET), STPS3H100 (diode, for D_1, D_2, and D_3), STTH3R02 (diode, for D_4, D_5, D_6, and D_7), STTH3R04 (diode, for D_8), STTH3R06 (diode, for D_o), and ETD 39 (core, for L_1, L_2, L_3, and L_4). For Fig. 16(e) [52] topology, components are IRFB4127 (MOSFET, for S_1 and S_2), STTH3R04 (diode, for D_{c1}, D_{c2}, D_{c3}, and D_{c4}), and EE42/21/20 (core, for L_1 and L_2). For Fig. 25 (f) [58] topology, components are IRFB4127 (MOSFET), STTH3R02 (diode, for D_{c1}), STTH3R06 (diode, for D_{C2} and D_o), and EE43/21/20 (core). Fo Fig. 26(d) [65] topology, components are are IRFB4127 (MOSFET), STTH3R02 (diode, for D_o), STTH3R06 (diode, for D_{C2} and D_{o2}), and EE43/21/20 (core). For Fig. 30(f) [98] and Fig. 31(c) [110] topologies, components are IRFB4710 (MOSFET), STPS3H100 (diode, for D_{c1}), STTH3R04 (diode, for D_{c2}, D_{c3}, D_o), and EE42/21/20 (core). For Fig. 34(c) [118] topology, components are IRFB4127 (MOSFET), STTH3R02 (diode, for D_{c1a} and D_{c1b}), STTH3R06 (diod, for D_{c2a}, D_{c2b}, D_{o1}, and D_{o2}), and EE42/21/20 (core, for T_{r1} and T_{r2}). For Fig. 36(b) [123] topology, components are IRFB4127 (MOSFET), STPS10H100 (diode, for D_1 and D_2), STTH3R02 (diode, for D_{c1}), STTH3R06 (diode, for D_{c2} and D_o), EC 52 (core, for L_{in} and Tr). For Fig. 39(b) [127] topology, components are IRFB4127 (MOSFET), STTH3R02 (diode, for D_{c1} and D_{c2}), STTH3R06 (diode, for D_{c3} and D_o), EE47/21/16 (core, for L_{in}), EE/35/24/10 (core, for Tr).

Table A Performance comparison of the converters with noncoupled inductor.

Topology		Componunt count (switch/diode/ capacitor /magnetic core)	Voltage gain/formula	Switch voltage stress/formula [V]	The maxsimum diode voltage stress/formula [V]	Soft switching	Experiments	
							Vin [V]/ Vout [V]/fs [kHz]/Pmax [kW]	Peak efficiency [%]
Basic step-up converters with switched inductor/capacitor cell	Fig. 6 (a) [13]	1/3/3/1	$7.5/\frac{2}{1-D}$	$\approx 50/\frac{V_o}{2}$	$\approx 50/\frac{V_o}{2}$	—	12/90/94/ 0.04	≈ 91.6
	Fig. 6 (c) [25]	1/5/5/1	$6/\frac{3}{1-D}$	$\approx 100/\frac{V_o}{3}$	$\approx 100/\frac{V_o}{3}$	—	50/300/100/ 0.14	≈ 89.6
	Fig. 6 (f) [21]	1/7/5/3	$12/\frac{5+D}{1-D}$	$66/\frac{3V_o}{5+D}$	$65/\frac{3V_o}{5+D}$	—	1015/120/ 20/0.475	≈ 92
Basic step-up converters with acrtive-passive switched inductor/capacitor cell	Fig. 8 (b) [22]	2/7/1/4	$10/\frac{1+3D}{1-D}$	$\approx 110/\frac{(2+2D)V_o}{2(1+3D)}$	$\approx 245/\frac{(2+2D)V_o}{1+3D}$	—	2040/200/ 50/0.2	≈ 95.9
	Fig. 8 (c) [23]	2/9/3/4	$20/\frac{3+5D}{1-D}$	$\approx 105/\frac{(2+2D)V_o}{2(3+5D)}$	$\approx 210/\frac{(2+2D)V_o}{3+5D}$	—	2040/400/ 100/0.2	≈ 95.5
Cascaded converters	Fig. 9 (b) [33]	1/3/2/2	$3.75/\frac{1}{(1-D)^2}$	V_o	V_o	—	48/150/20/ 0.1	94
	Fig. 9 (d) [32]	1/3/2/2	$4/\frac{1}{(1-D)^2}$	V_o	V_o	—	50/200/70/ 0.067	96.2
	Fig. 9 (e) [10]	1/5/4/3	$10/\frac{1}{(1-D)^2}$	V_o	V_o	ZVT	3050/300/ 50/0.3	93.42
Cascaded converters with switched inductor/capacitor	Fig. 11(c) [37]	1/8/6/3	$33/\left(\frac{2-D}{1-D}\right)^3$	$-/\frac{V_o}{2-D}$	$-/\frac{V_o}{2-D}$	—	20/660/100/ 0.015	78
Stacked converters	Fig. 14(a) [46]	2/2/2/1	$\frac{2}{1-D}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	—	198/400/40/ 2	≈ 93
	Fig. 14(b) [46]	2/8/6/1	$\frac{2}{1-D}$	$\frac{V_o}{2}$	—	ZVS turn-off, ZCS turn-on	198/400/40/ 2	≈ 94.4
Interleaved converters with voltage multiplier cell	Fig. 16(a) [49]	2/4/3/2	$8.33/\frac{2}{1-D}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	—	24/200/40/ 0.4	≈ 92.7
	Fig. 16(b) [50]	2/4/4/2	$14.58/\frac{4}{1-D}$	$\approx 100/\frac{V_o}{4}$	$\approx 200/\frac{V_o}{2}$	—	24/350/60/ 0.175	—
	Fig. 16(e) [52]	2/4/5/2	$20/\frac{4}{1-D}$	$\approx 100/\frac{V_o}{4}$	$\approx 200/\frac{V_o}{2}$	—	20/400/100/ 0.4	94.6

Table B Performance comparison of the stacked coupled inductor high step-up converters.

Topology			Componunt count (switch/diode/ capacitor/ magnetic core)	Voltage gain/formula	Switch voltage stress/formula [V]	The maxsimum diode voltage stress/formula [V]	Soft switchin	Experiments	
								Vin [V]/Vout [V]/ fs [kHz]/Pmax [kW]	Peak Efficiency [%]
Boost converters with stacked coupled inductor at input section		Fig. 25 (a) [57]	1/3/3/1	$14.81/\frac{1+n_3}{1-D}+1+n_2$	$\approx 58\,\frac{V_o}{(2+(1-D)n_3+(n_2-1)D)}$	$\approx 290\,\frac{(1+n_2)V_o}{(2+(1-D)n_3+(n_2-1)D)}$	—	27 36.5/400/100/ 0.3	95.2
		Fig. 25 (c) [60]	1/4/4/1	$6.67/\frac{2-D+n_3}{1-D}+1+n_2$	$120\,\frac{V_o}{(1-D)n_2+n_3+2-D}$	$-\frac{(1+n_2)V_o}{(1-D)n_2+n_3+2-D}$	—	60 90/400/50/2	96.81
		Fig. 25 (f) [58]	1/3/3/1	$16/\frac{1+n}{1-D}$	$87/\frac{V_o}{1+n}$	$350/\frac{nV_o}{1+n}$	ZCS turn-on and turn-off	25 50/400/50/0.4	97
		Fig. 25 (g) [56]	2/4/4/1	$13.33/\frac{1+n+D}{1-D}$	$\approx 86/\frac{V_o}{1+n+D}$	$\approx 260/\frac{nV_o}{1+n+D}$	—	30 50/400/50/0.5	96.4
		Fig. 25 (l) [55]	2/3/3/1	$19/\frac{(1+2n)D+1}{1-D}$	$\approx 105/\frac{V_o}{(1+2n)D+1}$	$\approx 420/\frac{2nV_o}{(1+2n)D+1}$	—	20 50/380/100/0.4	≈ 96.4
Boost converters with stacked coupled inductor at output section		Fig. 26 (c) [63]	1/3/3/1	$8.33/\frac{1+n}{1-D}$	$-/\frac{V_o}{1+n}$	$-/\frac{nV_o}{1+n}$	—	48/400/20/0.3	—
		Fig. 26 (d) [65]	2/2/3/1	$9.53/\frac{1+n}{1-D}$	$\approx 120/\frac{V_o}{1+n}$	$\approx 280/\frac{nV_o}{1+n}$	ZVT	42/400/70/0.25	96
		Fig. 26 (f) [68]	1/6/6/1	$16.67/\frac{1+2n+nD}{1-D}$	$60.04/\frac{V_o}{1+2n+Dn}$	$\approx 150/\frac{nV_o}{1+2n+Dn}$	—	24/400/50/0.2	95.31
Converters with low input current ripple	Converters with interleaved structure	Fig. 27 (b) [72]	2/6/5/2	$7.92/n_2+\frac{(2n_3-1)+2}{1-D}$	$\approx 86/\frac{V_o}{2-Dn_2-n_2+D(2n_3-1)}$	$\approx 250/\frac{(n_3+1)V_o}{2-Dn_2-n_2+D(2n_3-1)}$	—	48/380/50/2	96.5
		Fig. 27 (d) [75]	2/4/4/2	$10/\frac{2+2n}{1-D}$	$\approx 100/\frac{V_o}{2+2n}$	$\approx 200/\frac{2nV_o}{2+2n}$	—	40/400/40/1	97.44
		Fig. 27 (e) [74]	4/3/4/2	$16.67/\frac{1+3n}{1-D}$	$\approx 70/\frac{V_o}{1+3n}$	$\approx 240/\frac{2nV_o}{1+3n}$	ZVT	24/400/50/0.8	95.6
		Fig. 27 (f) [76]	2/4/4/2	$10/\frac{2+2n}{1-D}$	$30/\frac{V_o}{2+2n}$	$\approx 200/\frac{2nV_o}{2+2n}$	—	12/120/50/0.14	96
	Converters with integrate Boost converter	Fig. 28 (a) [80]	1/4/3/2	$20/\frac{1+nD}{(1-D)^2}$	$\approx 120/\frac{V_o}{1+nD}$	$-/\frac{nV_o}{1+nD}$	—	20 40/400/40/0.2	93.3
	Sepic converter with coupled inductor	Fig. 29 (a) [82]	2/2/4/2	$10/\frac{1+n}{1-D}$	$\approx 50/\frac{V_o}{1+n}$	$\approx 200/\frac{nV_o}{1+n}$	ZVT	24/*150 ~ 250*/85/ 0.135	94 95
		Fig. 29 (b) [83]	1/3/4/2	$11.11/\frac{1+n}{1-D}$	$\approx 50/\frac{V_o}{1+n}$	$\approx 160/\frac{nV_o}{1+n}$	—	18 30/200/100/ 0.16	96 97

Table C Performance comparison of the cascaded coupled inductor high step-up converters.

Topology			Componunt count (switch/diode/capacitor /magnetic core)	Voltage gain/formula	Switch voltage stress/formula [V]	The maxsimum diode voltage stress/formula [V]	Soft switching	Experiments	
								Vin [V]/Vout [V]/fs [kHz]/ Pmax [kW]	Peak efficiency [%]
Boost converters with cascaded coupled inductor to input section		Fig. 30(c) [93]	1/3/3/1	$16/\frac{2+n}{1-D}$	$\approx 50/\frac{V_o}{2+n}$	$\approx 340/\frac{(n+1)V_o}{2+n}$	—	25 38/400/100/ 0.25	97.4
		Fig. 30(e) [98]	1/4/4/1	$10/\frac{2+n+nD}{1-D}$	$\approx 80/\frac{V_o}{2+n+nD}$	$\approx 230/\frac{(n+1)V_o}{2+n+nD}$	—	40/400/60/0.3	96.9
		Fig. 30 (g) [100]	1/5/5/1	$33.33/\frac{3+n(2+D)}{1-D}$	$\approx 23/\frac{V_o}{3+n(2+D)}$	$\approx 178/\frac{(n+1)V_o}{3+n(2+D)}$	—	12/400/45/0.2	96.89
		Fig. 30(l) SPS: refid:: bib101 [101]	1/4/4/1	$10/\frac{2+n+nD}{1-D}$	$\approx 40/\frac{V_o}{2+n+nD}$	$\approx 135/\frac{(n+1)V_o}{2+n+nD}$	—	20/200/50/0.2	97.1
		Fig. 30 (n) [85]	1/3/3/1	$20/\frac{2n_{12}+n_{32}-1}{(1-D)(n_{12}-1)}$	$\approx 60/\frac{2n_{12}-1}{n_{12}+n_{32}-1}$	$\approx 380/\frac{(n_{12}+n_{32})V_o}{n_{12}+n_{32}-1}$	—	20 40/400/100/ 0.4	97.7
		Fig. 32 (b) [95]	2/2/3/1	$19/\frac{2+n}{1-D}$	$-/\frac{V_o}{2+n}$	$-/\frac{(n+1)V_o}{2+n}$	ZVT	20 45/380/100/ 0.25	97.7
		Fig. 33 (a) [89]	2/2/3/1	$11.88/\frac{1+n_2+n_3}{1-D}+2n_2+n_3+2$	$-/\frac{V_o}{(3+3n_2+2n_3-D(2n_2+n_3+2))}$	$-/V_o-\frac{V_o(1-D)}{(3+3n_2+2n_3-D(2n_2+n_3+2))}$	ZVT	16 24/190/80/ 0.152	95.6
Boost converters with cascaded coupled inductor to output section		Fig. 31 (a) [108]	1/2/2/1	$8.33/\frac{1+nD}{1-D}$	$\approx 70/\frac{V_o}{1+nD}$	$-/\frac{nV_o}{1+nD}$	—	24/200/100/0.2	≈ 94
		Fig. 31(c) [110]	1/4/4/1	$16.67/\frac{1+n}{1-D}+n$	$64/\frac{V_o}{1+2n-nD}$	$\approx 245/\frac{nV_o}{1+2n-nD}$	—	24/400/50/0.4	96.8
		Fig. 31(e) [87]	2/2/2/1	$10/\frac{2nD+D+1}{1-D}$	$\approx 50/\frac{V_o}{2nD+D+1}$	$\approx 250/\frac{(2n+1)V_o}{2nD+D+1}$	—	20/200/50/0.2	95.9
Converters with low input current ripple	Converters with interleaved structure	Fig. 34 (a) [114]	4/2/3/2	$9.5/\frac{1+n}{1-D}$	$\approx 170/\frac{V_o}{1+n}$	$-/\frac{2nV_o}{1+n}$	—	38 50/380/50/2	93.9
		Fig. 34(c) [118]	2/6/5/2	$18.25/\frac{2(1+n)}{1-D}$	$96/\frac{V_o}{2(1+n)}$	$\approx 260/\frac{(2n+1)V_o}{2(1+n)}$	ZVS turn-off and ZCS turn-on	20 30/365/50/1	97.2

(*continued on next page*)

Table C (*continued*)

Topology			Componunt count (switch/diode/ capacitor /magnetic core)	Voltage gain/formula	Switch voltage stress/formula [V]	The maxsimum diode voltage stress/formula [V]	Soft switching	Experiments	
								Vin [V]/Vout [V]/fs [kHz]/ Pmax [kW]	Peak efficiency [%]
		Fig. 35 (b) [113]	2/4/3/2	$9.5/\frac{1+2n}{1-D}$	$\approx 140/\frac{V_o}{1+2n}$	$\approx 250/\frac{2nV_o}{1+2n}$	ZCS turn-on	40/380/100/1	94.7
		Fig. 34(e) [119]	2/4/4/2	$20/\frac{4+2n}{1-D}$	$\approx 68/\frac{V_o}{4+2n}$	$\approx 266/\frac{(n+1)V_o}{2+n}$	ZCS turn-on	20/400/50/0.33	95.1
	Converters with integrated Boost converter	Fig. 36 (b) [125]	1/5/4/2	$21.11/\frac{2+n}{(1-D)^2}$	$\approx 90/\frac{V_o}{2+n}$	$\approx 280/\frac{(1+n)V_o}{2+n}$	—	18 36/380/40/ 0.5	94
		Fig. 36(c) [86]	1/5/4/2	$10/\frac{2n_2+n_3-1}{(n_2-1)(1-D)^2}$	$-/\frac{(n_2-1)V_o}{2n_2+n_3-1}$	$-/\frac{(n_2+n_3)V_o}{2n_2+n_3-1}$	—	38/380/50/0.4	96
	Sepic converter with coupled inductor	Fig. 37 [126]	1/3/4/2	$10.85/\frac{1+n}{1-D}$	$\approx 90/-$	$\approx 440/-$	ZVS turn-off	35/380/60/0.2	≈ 95
		Fig. 38 (a) [124]	1/3/4/2	$16.67/\frac{1+n}{1-D}$	$\approx 90/\frac{V_o}{1+n}$	$\approx 340/\frac{nV_o}{1+n}$	—	24/400/100/0.2	96.16
		Fig. 39 (b) [127]	1/4/5/2	$10/\frac{2+n+D}{1-D}$	$\approx 75/\frac{V_o}{2+n+D}$	$\approx 200/\frac{(n+1)V_o}{2+n+D}$	—	26/300/30/0.26	≈ 96.2

Table D Performance comparison of the Interleaved and inter-coupled boost converters.

Topology		Componunt count (switch/diode/capacitor /magnetic core)	Voltage gain/formula	Switch voltage stress/formula [V]	The maxsimum diode voltage stress/formula [V]	Soft switching	Experiments	
							Vin [V]/Vout [V]/ fs [kHz]/Pmax [kW]	Peak efficiency [%]
Interleaved and Intercoupled boost converter	Fig. 40 (a) [129]	2/2/1/1	$-/\frac{1}{1-2D}$	$-/V_0$	$-/V_0$	ZCS turn-on	—	—
	Fig. 40 (b) [130]	3/2/1/2	$2.5/\frac{1}{1-2D}$	$-/V_0$	$-/V_0$	ZVT and ZCS turn-on	100/250/50/0.5	95.12
	Fig. 40 (c) [131]	2/4/3/1	$9.5/\frac{1}{(1-D)D}$	—			12/48/50/0.06	≈ 87.5
	Fig. 40 (e) [133]	1/5/5/1	$9.5/\frac{4}{1-D}$	$9.5/\frac{V_0}{2}$	$-/V_0$	—	40 70/380/40/1.1	92

Table E Comparison of the representative topologies selected among the above overviewed converters with coupled inductor ($P_o = 200\ W,\ V_{in} = 25\ V,\ V_o = 400\ V, f_s = 50\ kHz$).

Chosen Topology		Componunt count (switch/diode/capacitor/ magnetic core)	Diodes Vpk, IRMS, Ipk, ScR	Switches Vpk, IRMS, Ipk, ScR	Magnetizing inductance, Turn ratio
Converters with coupled inductor	Fig. 25 (f) [58] (Boost converter with stacked coupled inductor at input section)	1/3/3/1	D_{c1}: 82.6 V, 1.797 A, 9.7 A D_{c2}: 318 V, 0.61 A, 0.834 A D_o: 318 V, 0.96 A, 2.2 A $\sum V_{pki}.I_{RMSi} = 647.7VA$	S: 84.1 V, 9.47 A, 14.7 A $\sum V_{pki}.I_{RMSi} = 796.4VA$	Lm = 54μH, 1:4
	Fig. 26 (d) [65] (Boost converter with stacked coupled inductor at output section)	1/3/3/1	D_{c2}: 321 V, 0.623 A, 0.87 A D_{o2}: 320 V, 0.93 A, 2.06 A D_o: 81.2 V, 1.56 A, 6.9 A $\sum V_{pki}.I_{RMSi} = 624.3VA$	S: 83.2 V, 9.27 A, 13.6 A $\sum V_{pki}.I_{RMSi} = 771.3VA$	Lm = 54μH, 1:4
	Fig. 30 (f) [98] (Boost converter with cascaded coupled inductor to input section)	1/4/4/1	D_{c1}: 52.1 V, 1.84 A, 19.8 A D_{c2}: 256 V, 0.78 A, 3.34 A D_{c3}: 255 V, 0.72 A, 1.35 A D_o: 255 V, 0.75 A, 1.42 A $\sum V_{pki}.I_{RMSi} = 670.4VA$	S: 52.9 V, 11 A, 21 A $\sum V_{pki}.I_{RMSi} = 581.9VA$	Lm = 54μH, 1:4
	Fig. 31 (c) [110] (Boost converter with cascaded coupled inductor to output section)	1/4/4/1	D_{c1}: 62.7 V, 1.7 A, 19.8 A D_{c2d}: 244 V, 0.686 A, 1.25A D_{c3u}: 244 V, 0.687 A, 1.24 A D_o: 244 V, 0.504 A, 1.62 A $\sum V_{pki}.I_{RMSi} = 564.6VA$	S: 63.7 V, 10.4 A, 18.5 A $\sum V_{pki}.I_{RMSi} = 662.5VA$	Lm = 62μH, 1:4
Coupled inductor converters with low input current ripple	Fig. 34 (c) [118] Interleaved converter	2/6/5/2	D_{c1a}, D_{c1b} = 100 V, 1.95 A, 8.98 A D_{c2a}, D_{c2b} = 300 V, 1.15 A, 2.83 A D_{o1}, D_{o2} = 300 V, 1.12 A, 3.26 A $\sum V_{pki}.I_{RMSi} = 876X2VA$	S_1, S_2 = 102 V, 9.5 A, 16.4 A $\sum V_{pki}.I_{RMSi} = 969X2VA$	Lm = 60μH, 1:1:1

(*continued on next page*)

Table E (*continued*)

Chosen Topology		Componunt count (switch/diode/capacitor/ magnetic core)	Diodes Vpk, IRMS, Ipk, ScR	Switches Vpk, IRMS, Ipk, ScR	Magnetizing inductance, Turn ratio
	Fig. 36 (b) [125] Converter with Integrated boost	1/5/4/2	D_1: 48.1 V, 6.33 A, 12.4 A D_2: 54.5 V, 6.8 A, 12.2 A D_{c2}: 296 V, 0.9 A, 2.24 A D_o: 296 V, 0.88 A, 1.19 A $\sum V_{pki}.I_{RMSi} = 1302.9VA$	S: 105 V, 11.8 A, 17.9 A $\sum V_{pki}.I_{RMSi} = 1239VA$	Lin:37μH, Lm:170uH, 1:1.86
	Fig. 39 (b) [127] Sepic converter with coupled inductor	1/4/5/2	D_{c1}: 86.2 V, 1.22 A, 3.86 A D_{c2}: 86.4 V, 1.43 A, 9.6 A D_{c3}: 254 V, 0.66 A, 1.1 A D_o: 254 V, 0.97 A, 2.19 A $\sum V_{pki}.I_{RMSi} = 642.7VA$	S: 86.7 V, 9.2 A, 12.8 A $\sum V_{pki}.I_{RMSi} = 797.6VA$	Lin:55μH, Lm:350uH, 1:2.1

Table F Comparison of the representative topologies selected among the above overviewed converters with noncoupled inductor ($P_o = 200\ W$, $V_{in} = 25\ V$, $V_o = 400\ V$, $f_s = 50\ kHz$).

Chosen Topology		Componunt count (switch/diode/capacitor/ magnetic core)	Diodes Vpk, IRMS, Ipk, ScR	Switches Vpk, IRMS, Ipk, ScR	Inductance
Converters with noncoupled inductor	Fig. 8 (c) [23] (Basic step-up converters with acrtive-passive switched inductor/capacitor cell)	2/9/3/4	D_{1a}, D_{3a}, D_{1b}, D_{3b}: 40.7 V, 2.4 A, 3.82 A D_{2a}: 23 V, 1.86 A, 3.82 A D_{c1}: 212 V, 0.972 A, 2.02 A D_{c2}: 212 V, 0.984 A, 3.5 A D_{c3}: 212 V, 1.14 A, 3.78 A $\sum V_{pki}.I_{RMSi} = 1047.1VA$	S1, S2: 108 V, 5.08 A, 7.62 A $\sum V_{pki}.I_{RMSi} = 1097.28VA$	$L_1 = L_2 = L_3 = L_4 = 145\mu H$
	Fig. 11 (b) [40] (Cascaded converters with switched inductor cell)	1/9/2/4	D_{1a}, D_{3a} = 32.8 V, 5.56 A, 8.63 A D_{2a}: 17.8 V, 4.15 A, 8.63 A D_{1b}, D_{3b}: 155 V, 1.18 A, 1.88 A D_{2b}: 84.5 V, 0.88 A, 1.88 A D_4: 85.4 V, 4.03 A, 8.6 A D_5: 310 V, 11 A, 17.2 A D_o: 400 V, 13.3 A, 21 A $\sum V_{pki}.I_{RMSi} = 9952.93VA$	S: 400 V, 13.3 A, 21 A $\sum V_{pki}.I_{RMSi} = 5320VA$	$L_1 = L_2 = 60\mu H$
	Fig. 16 (e) [52] (Interleaved converters with voltage multiplier cell)	2/4/5/2	D_{c1}: 200 V, 2.1 A, 4.65 A D_{c2}: 200 V, 2.15 A, 6.2 A D_{c3}: 200 V, 2.24 A, 7.65 A D_{c4}: 200 V, 2.12 A, 5.38 A $\sum V_{pki} \cdot I_{RMSi} = 861X2VA$	S_1, S_2 = 103 V, 10.6 A, 19.3 A $\sum V_{pki}.I_{RMSi} = 1091.8X2VA$	$L_1 = L_2 = 60\mu H$

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